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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT.(U)
SEP 76 J E BREWER, T G O'DONNELL, P C SMITH DAAB07-76-C-0048
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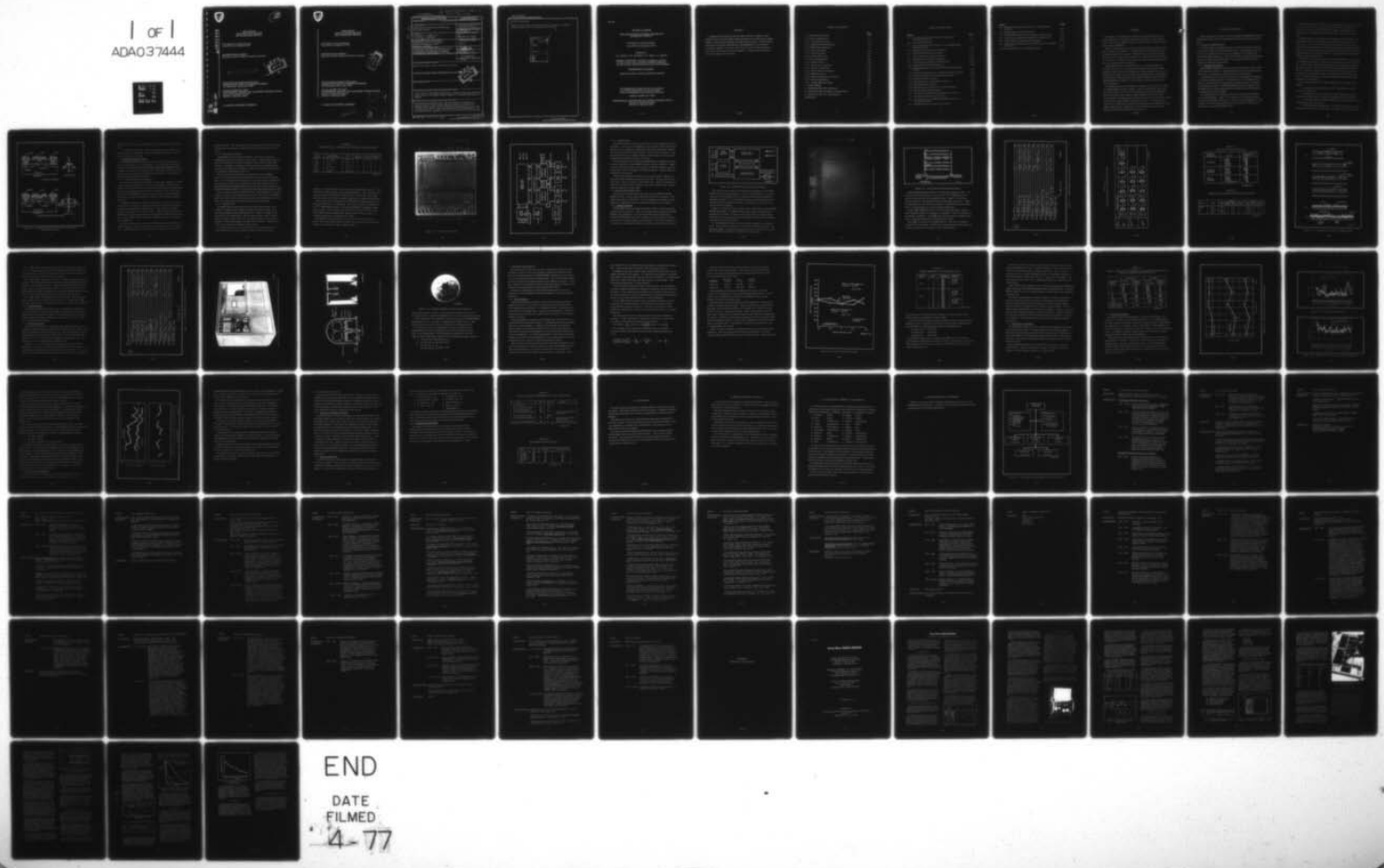

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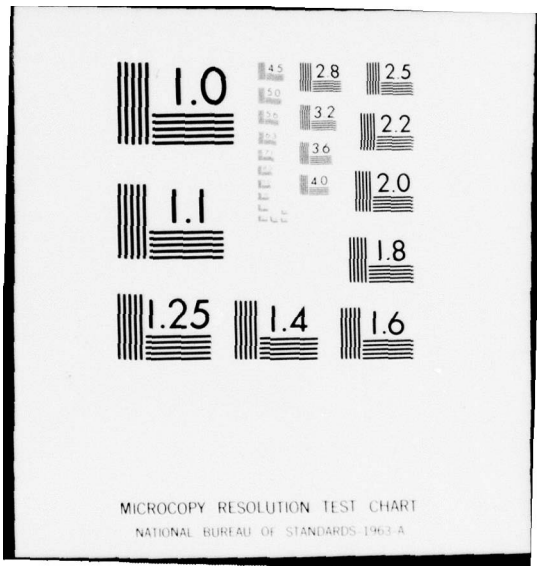
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MNOS BORAM
MANUFACTURING METHODS
AND TECHNOLOGY PROJECT

First Quarterly Progress Report
1 July 1976 to 30 September 1976

DISTRIBUTION STATEMENT
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Procurement and Production Directorate
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Fort Monmouth, New Jersey 07703

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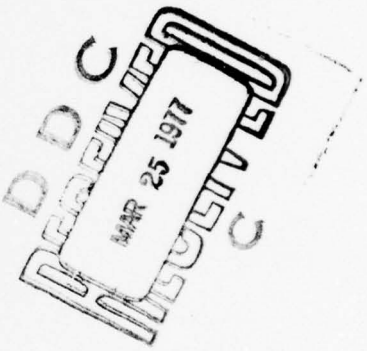

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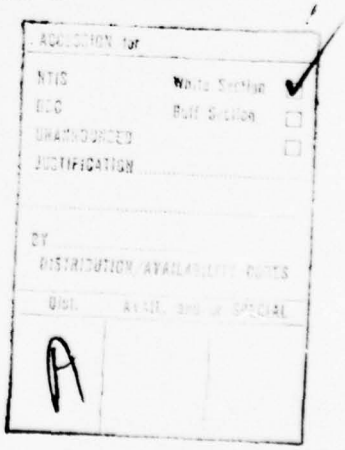

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A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductors (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. The first phase of activity is concerned with definition and establishment of the required production capability. This report describes the chip fabrication

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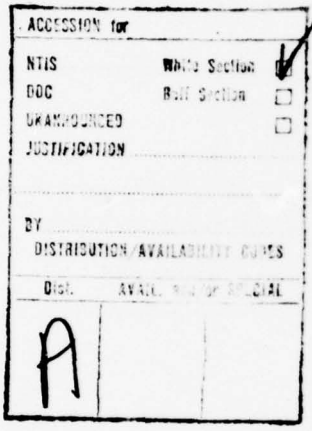
sequence, and outlines some experimental investigations. Program status and plans for the next quarter are reviewed.



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TECHNICAL REPORT

MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

First Quarterly Progress Report

1 July 1976 to 30 September 1976

Prepared by

J.E. Brewer, T.G. O'Donnell, P.C. Smith, L.A. Epstein

PROJECT OBJECTIVE: Establish a production capability for metal nitride oxide semiconductor (MNOS) integrated circuits for block oriented random access memory (BORAM).

Contract DAAB07-76-C-0048

WESTINGHOUSE DEFENSE AND ELECTRONICS SYSTEMS CENTER
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ABSTRACT

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductors (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. The first phase of activity is concerned with definition and establishment of the required production capability. This report describes the chip fabrication sequence, and outlines some experimental investigations. Program status and plans for the next quarter are reviewed.

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PURPOSE

The purpose of manufacturing method and technology (MM&T) project number 2769758 is to establish a production capability for metal nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM hold considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. (See the appendix for a description of the module.) When compared to fixed-head electromechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times about 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuits per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronic Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Procurement Requirement Number 15.

1. NARRATIVE AND DATA

This first quarterly technical report on the MNOS BORAM MM&T project describes the device and the related state of the art at the start of the program.

1.1 DEVICE CONSIDERATIONS

The end product of the MM&T project is a 16-chip hybrid micrccircuit. Each chip is a 2048-bit MNOS integrated circuit. The emphasis of the project is on the achievement of low cost manufacture of this relative fast read/write MNOS component. This report provides background information on chip manufacturing considerations. Later reports will examine the details of hybrid circuit fabrication.

1.1.1 Transistor Structures

MNOS BORAM integrated circuits used during this project contain about 5000 transistor structures. Understanding and control of transistor characteristics is fundamental to achievement of the project goals.

An MNOS nonmemory transistor performs the same type of functions as a conventional MOS transistor. The physical form of the MNOS device is similar to the MOS device, except that the insulator region is composed of two dielectric layers. The MNOS BORAM nonmemory transistor has 800 angstroms of oxide (SiO_2) adjacent to the silicon, and 450 angstroms of nitride (Si_3N_4) over the oxide.

Two types of memory transistors have been used in previous MNOS work at Westinghouse. Figure 1-1 compares the so called unprotected and protected transistor structures. The major physical difference is that the thin 15 to 25 Å tunneling oxide does not overlap the P+ diffusions in the drain source protected (DSP) device.

Unprotected transistors exhibit severe degradation with use. After about 10^6 erase-write cycles the V_{HC} and V_{LC} states cannot be distinguished. This class of transistor is also difficult to employ in integrated circuit arrays because of depletion mode operation while in the high conduction state.

The DSP transistor was invented at Westinghouse by J.R. Cricchi. It has been shown to provide reliable memory operation beyond 10^{11} erase-write cycles. The central device design concept was to protect the thin oxide from stresses associated with material imperfections and/or electric fields. The thick nonmemory oxide employed close to the source and drain determines the gate breakdown potential. Junction fields do not affect the stability of the tunneling oxide.

The DSP device can be thought of as a memory transistor in series with two nonmemory transistors as shown in the equivalent circuit of figure 1-4 (B). The P-channel enhancement mode nonmemory transistors determine the high conductance state of the DSP structure, and therefore, the DSP device is confined to enhancement mode operation. In large integrated arrays this is an important feature. Interconnection schemes for erase, write, read and standby can be achieved without contending with difficult parasitic current problems.

Some of the advantages of the DSP transistors can be summarized as follows:

a. Reliable memory operation for $> 10^{11}$ high field erase write cycles can be achieved

b. Enhancement mode operation allows the parallel connection of transistors in large arrays in a manner compatible with read circuitry

c. Drain and source breakdown voltages are increased to that of conventional nonmemory transistors

d. DSP transistor gate capacitance is reduced to about 25 percent of unprotected transistor gate capacitance. This allows four times as many

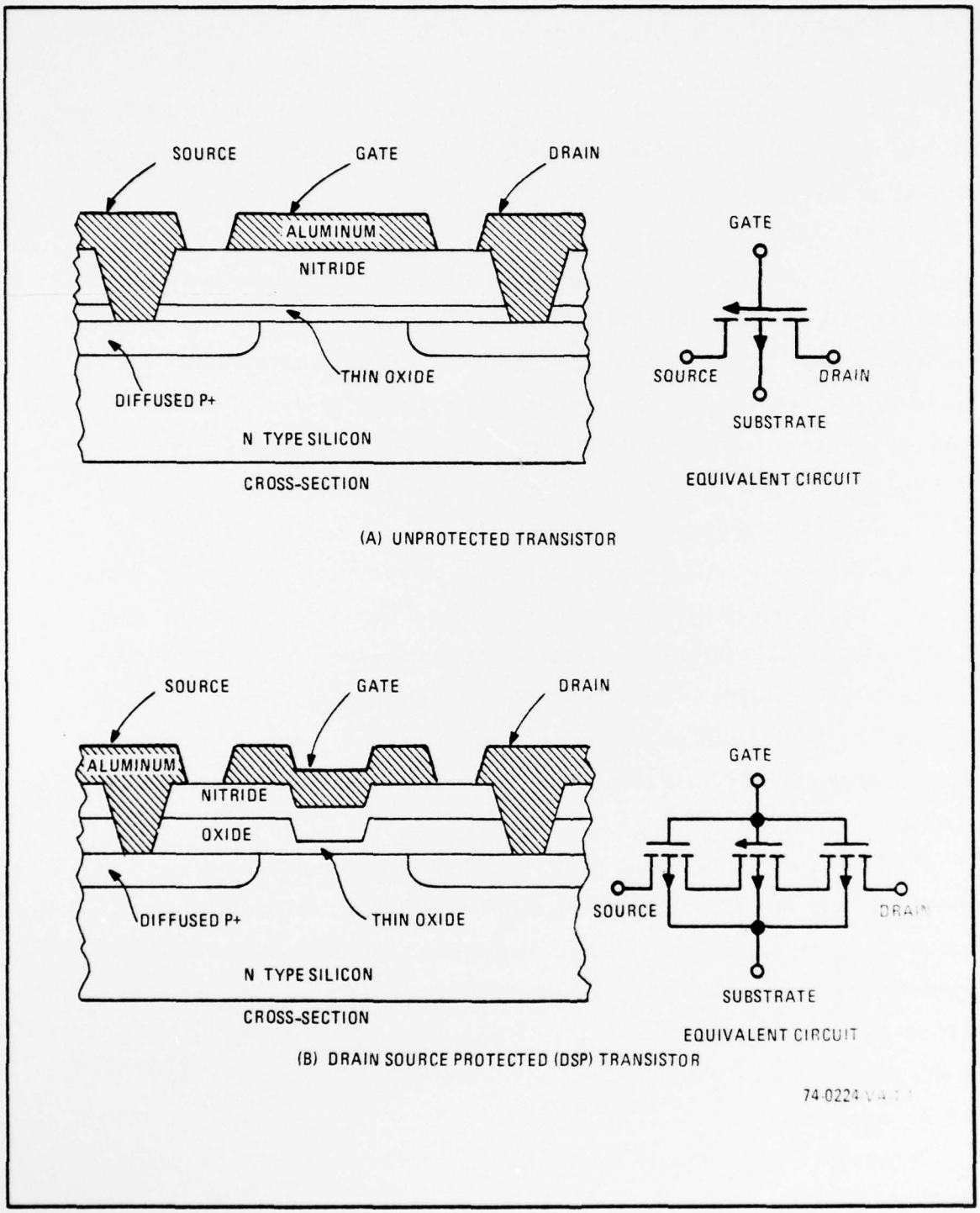

Figure 1-1. Comparison Between Protected and Unprotected Transistor Structures

DSP devices to be driven in parallel in an array with equivalent response times

e. DSP transistor gate to source capacitance is much smaller than that of unprotected transistors. Address voltage feedthrough to memory detection circuitry is reduced.

1.1.2 BORAM Integrated Circuits

At Westinghouse, BORAM integrated circuit development has been concurrent with memory system development. As a result the best characteristics of the MNOS technology have been intelligently applied to achieve computer secondary storage requirements. Chip design considerations will now be briefly reviewed, and the two integrated circuits to be fabricated during this project will be described.

1.1.2.1 Chip Organizational Advantages

To achieve cost effective performance, a solid state computer secondary storage unit must provide fast write and read capability. RAM organized MNOS electrically alterable memory chips are incompatible with this application because millisecond write times are required. To overcome this limitation, MNOS BORAM chips are designed for 10 to 100 microsecond write times, and operate in parallel on blocks of data to provide adequate data rates.

A BORAM chip contains a fully decoded random access memory, and a shift register for data I/O. A single read or write involves the transfer of many bits in parallel into the shift register. The contents of the shift register may be shifted at megahertz rates. This arrangement allows the MNOS RAM to operate at modest speeds compatible with high-yield production, while the shift register maintains the high-bit transfer rate required by the application.

Experience with volatile semiconductor RAM production has shown that yield to dynamic response criteria such as access time is a major impact item. MNOS BORAM devices should suffer very little production loss to

dynamic criteria. The chip circuitry when operating in a secondary storage unit will never be required to operate near the performance limits of the device.

1.1.2.2 Chip Design Evolution

MNOS BORAM chip development has been a process of continuous simplification and refinement over several years. Initial designs required two level metalization and single transistor cells to achieve produceable die sizes. Attempts to manufacture these devices led to identification of critical circuit and process problems. Successive designs eliminated and/or avoided these difficulties (table 1-1).

The most successful design prior to this project was the BORAM 6000C. It employs a single-level metal interconnect and a two transistor cell. The two-transistor cell has proven to be a major factor in high-yield production in the presence of variability of transistor characteristics. It has also improved the opportunities for thorough test of the memory array, and provides longer effective data retention times than single transistor cells.

Recent design studies have identified ways of achieving smaller cell sizes without resorting to yield impacting layout rules. As a result, the BORAM 6002 chip which has only 46 percent of the area of the 6000C has been established. It is this device which will be placed in pilot production.

1.1.2.3 BORAM 6000C

The 6000C chip provides 2048 bits of nonvolatile data storage. It is intended for application in computer secondary storage systems, and is normally packaged in multi-chip hybrid form. Figure 1-2 shows the die and identifies the bonding pads. Pads are greater than 5 mils^2, and are located on opposite sides of the die. The chip measures 163 by 169 mils. A glass overcoat guards against scratches due to handling. Protective devices on all inputs avoid damage by static charge.

As shown in figure 1-3, the chip contains a fully decoded 64-word by 32-bit random access memory and two dynamic 2-phase 16-bit shift

TABLE 1-2

CHIP EVOLUTION - PROCESS AND TOPOLOGY SIMPLIFICATION

DEVICE NUMBER	FIELD THRESHOLD SUPPRESSION APPROACH	DIE SIZE mils	MASKING OPERATIONS	METAL LAYERS	TRANSISTORS PER CELL
6000	Nitride field shield	154 x 175	11	2	1
6000A	Nitride field shield	154 x 170	12	2	1
6000A	Ion implant	154 x 170	12	2	1
6000B	Channel stoppers	151 x 169	8	1	1
6000C	Channel stoppers	163 x 169	8	1	2
6002	Ion Implant	99 x 128	9	1	2

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registers. All data I/O takes place serially through the shift registers. The RAM and the shift registers may operate independently. Data is transferred in parallel between the RAM and registers via a 32-bit latch. Data output drivers are three-state devices capable of sinking a low power Schottky load.

When written with a 100-microsecond $\overline{MW}$ pulse the 6000C minimum unpowered retention time is 4000 hours. Data may be accessed a minimum of 2×10^{11} times without refresh. The chip is intended to be used as a read/write memory, and it may be erased and written at least 10^{10} times. In a normal BORAM system application, it would require about 100 years of continuous operation to accumulate 10^{10} cycles.

The 6000C has been operated over the -55°C to +125°C temperature range. The circuit design tolerates changes due to temperature and is also insensitive to variations in power supply voltages.

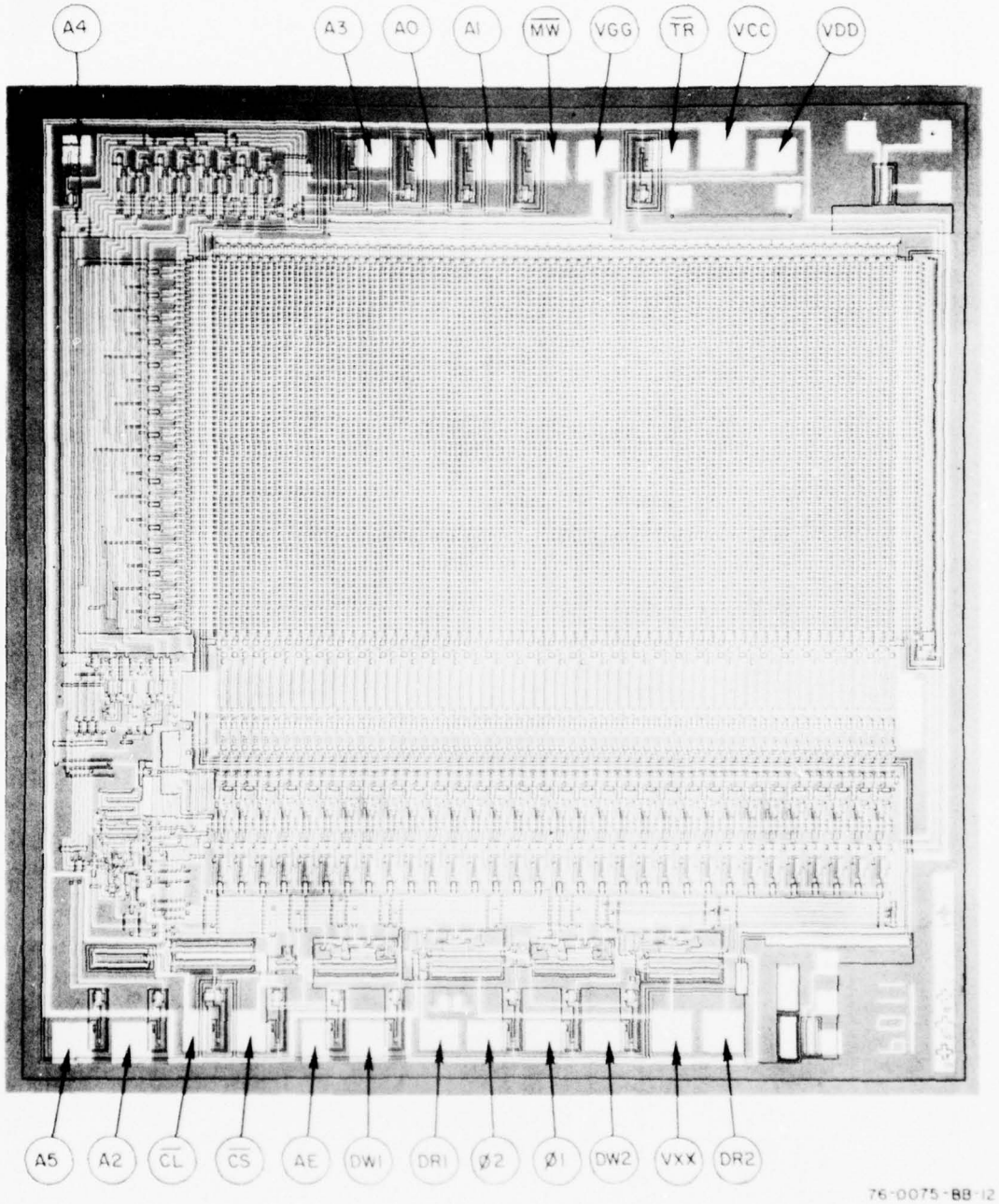

Figure 1-2. The BORAM 6000C Die

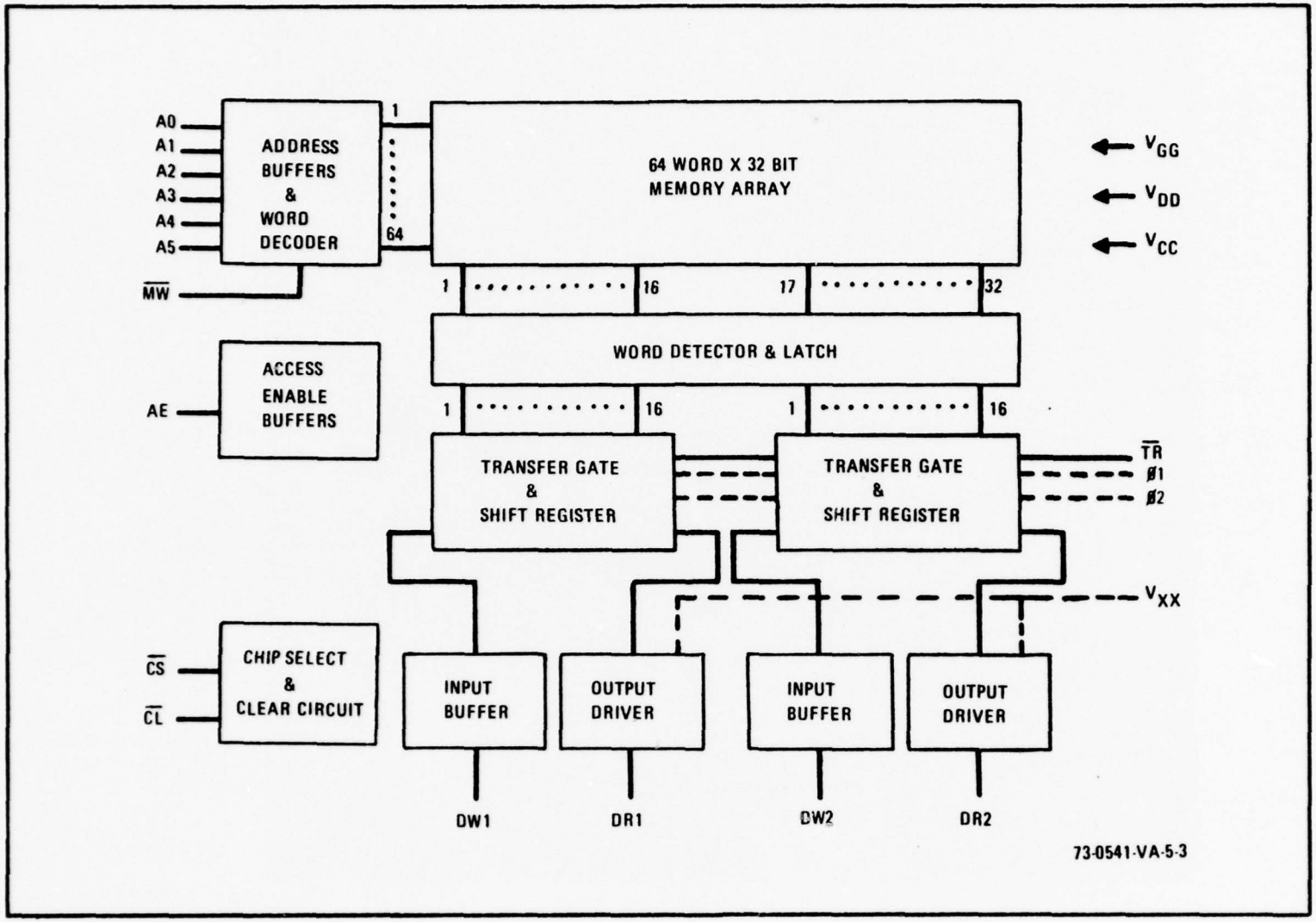

Figure 1-3. Structure Oriented Block Diagram of the BORAM 6000C Integrated Circuit

1.1.2.4 BORAM 6002

The 6002 design has resulted from studies of how to simplify and shrink the 6000C. From a process viewpoint, it was decided that the added complexity of an ion implant to establish field thresholds would save sufficient die area to provide a net cost reduction. From a layout viewpoint, it was noted that the use of two address decoders with interleaved row geometry would greatly reduce the memory array area.

Circuit functions were studied to establish whether simplification could save die area and/or reduce BORAM memory system complexity. Figure 1-4 shows that the revised circuit uses one 32-bit shift register, and requires only 15 pins. All inputs are CMOS compatible. Address inputs are multiplexed to save pins.

The die area reduction effort has been very successful. Figure 1-5 shows the metal interconnect pattern for the chip. The die measures 128 by 99 mils. This is 46 percent of the 6000C area. Major cost savings are expected to result because of greatly increased yield percentages, and because of many more die per wafer.

1.2 BORAM CHIP FABRICATION

The previous discussion has treated the nature of MNOS and MNOS BORAM devices. Now the fabrication sequence will be considered. The 6000C chip will be reviewed first. Process changes for the 6002 are then explained. Finally the memory insulator processing will be examined.

1.2.1 6000C Processing

BORAM 6000C chips are fabricated using a simple 7-active mask plus scratch protection process. This is the simplest known approach to MNOS BORAM chip manufacture, and has demonstrated high yield potential. Finished MNOS BORAM parts have a single level of metal for interconnection and use N+ channel stoppers in field regions. The process sequence is a variation of conventional P-channel enchancement mode MOS processing.

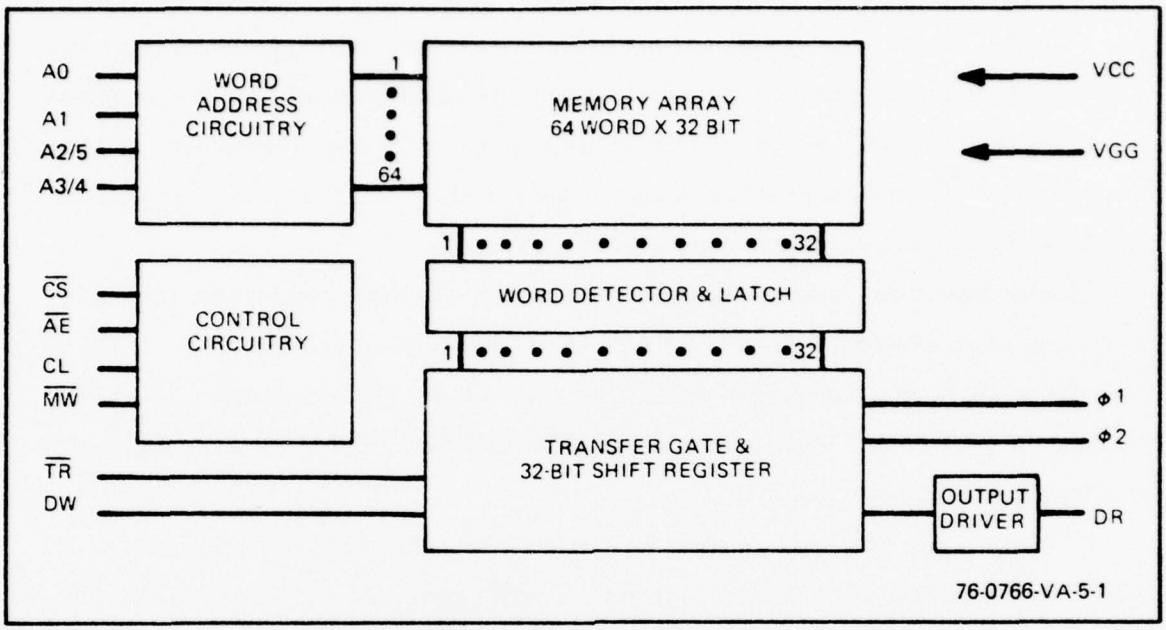

Figure 1-4. BORAM 6002 Functional Block Diagram

Two objectives were kept in mind during the development of the MNOS BORAM wafer processing sequence. The first was simplicty -- reduce the sequence to the minimum number of maskings and avoid yield impacting topological features. The second objective was to use only well known and characterized individual process steps. By doing this, the risks in line startup would be minimal.

Figure 1-6 provides a simple concept of how material flows during MNOS BORAM fabrication. The characteristic cyclic nature of semiconductor manufacture is evident. A wafer is first prepared by some photo and/or chemical process step, and then it is given some treatment which modifies the surface structure of the wafer.

The modification operations are oxide growth, diffusions, and depositions. These stations see the wafer only one time during fabrication. The photolithographic, etching and cleaning processes see the wafer many times. Photo processing experiences the highest work load volume.

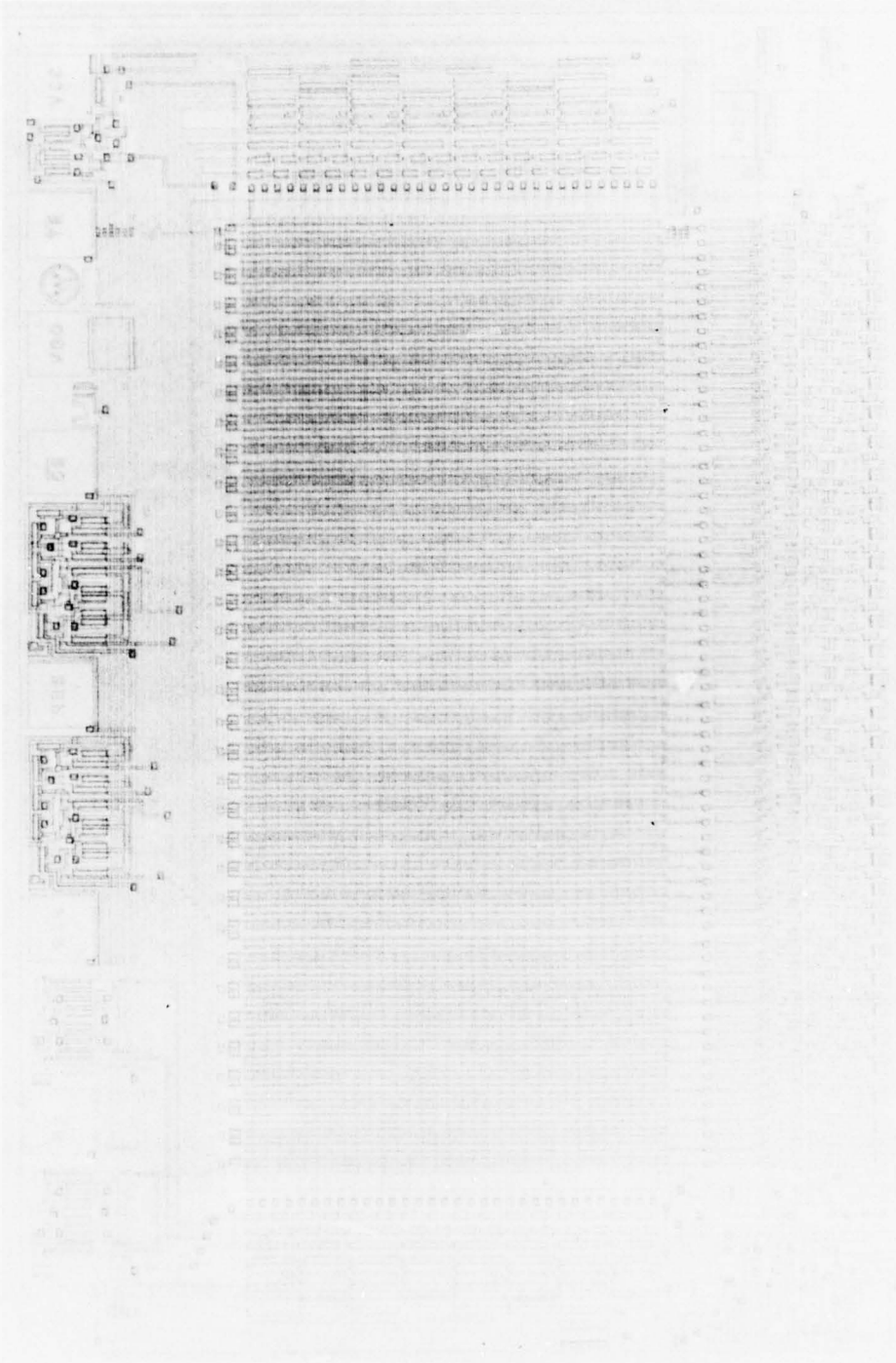

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Figure 1-5. BORAM 6002 Interconnect Pattern

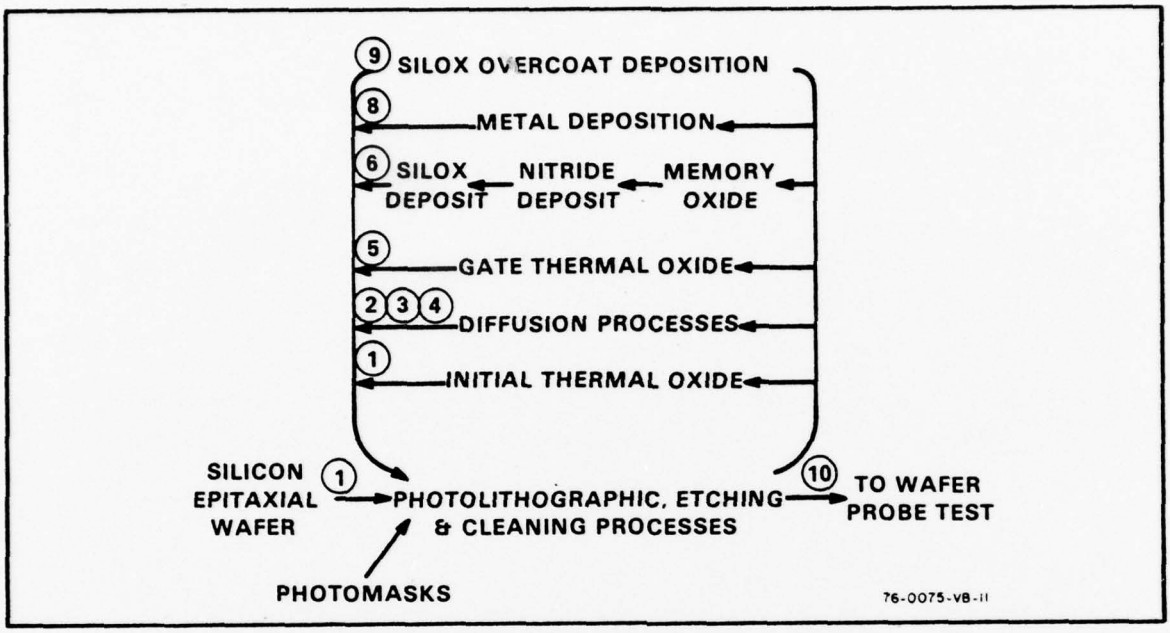

Figure 1-6. Cyclic Wafer Processing Flow Pattern

MNOS BORAM starting material is a <100> silicon epitaxial wafer. The substrate is 20 to 40 ohm cm. An N type 10^{15} cm^{-3} epitaxial layer 14 microns thick exists on the processing surface. Figure 1-7 shows the process sequence. Cleaning processes are described in table 1-2. Figure 1-8 illustrates how the wafer cross section is modified after various steps. Table 1-3 summarizes the various insulator thicknesses.

Cycles (1) to (4) form the P^-, N^+ and P^+ diffused layers. Conventional deposition and drive sequences are employed. Table 1-4 summarizes the diffusion conditions. Cycle (5) forms the non-memory transistor gate oxide. This heat treatment also continues the P^+ drive.

Cycle (6) is the heart of the MNOS process. The memory oxide and nitride layers are formed. Control of the tunneling oxide and the nitride are critical to achievement of proper memory characteristics.

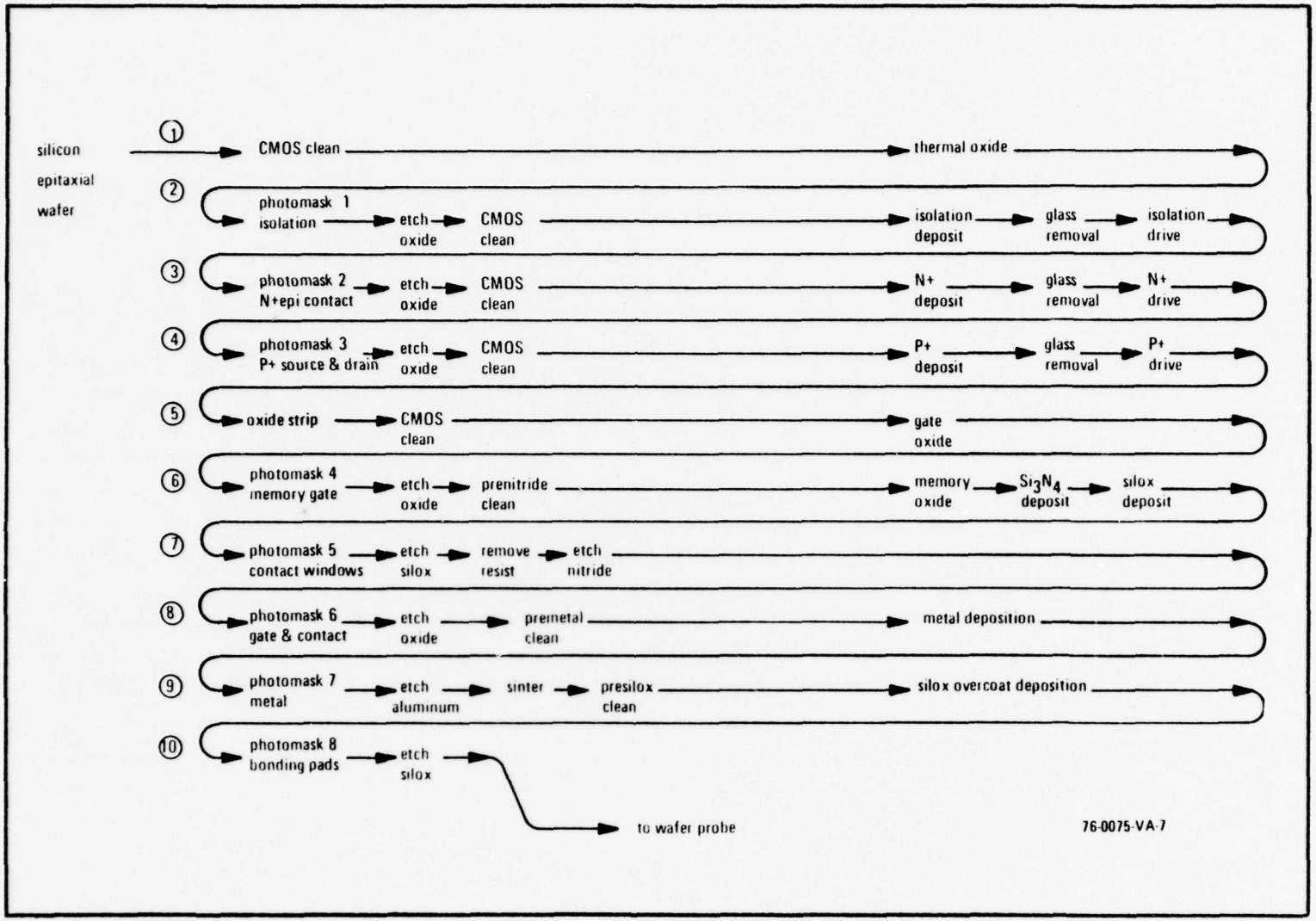

Figure 1-7. BORAM 6000C Fabrication Sequence

TABLE 1-2

MNOS BORAM 6000C CLEANING PROCESSES

Process	Sequence of Operations
CMOS Clean	H_2SO_4 175°C 10 min → DI Rinse 25°C → HNO_3 80°C 15 min → DI Rinse 25°C → HF 10:1 15 sec → DI Rinse 25°C → DI Rinse 100°C → Dist H_2O Rinse 25°C
Pre-Nitride Clean	H_2SO_4 175°C 10 min → DI Rinse 25°C → HNO_3 80°C 15 min → DI Rinse 25°C → HF 100:1 60 sec → DI Rinse 25°C
Pre-Metal Clean	H_2SO_4 175°C 10 min → DI Rinse 25°C → HNO_3 80°C 15 min → DI Rinse 25°C → HF 10:1 15 sec → DI Rinse 25°C

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TABLE 1-3

MNOS BORAM 6000C STRUCTURE

Topological Region of Chip	Material	Nominal Thickness (angstroms)
Field Region	• Silox • Metal • Silox • Nitride • Oxide	10,000 10,000 8,000 450 800
Nonmemory Gate Region	• Silox • Metal • Nitride • Oxide	10,000 10,000 450 800
Memory Gate Region	• Silox • Metal • Nitride • Tunneling Oxide	10,000 10,000 450 ~020

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TABLE 1-4

SUMMARY OF DIFFUSION STEPS FOR MNOS BORAM

Diffusion	Dopant	Deposition				Drive		
		Temp (°C)	Preheat (minutes)	Dep (minutes)	Flush (minutes)	Temp (°C)	Wet (minutes)	Dry (minutes)
Isolation	Boron	1150	5	30	1	1200	10	510
N+	Phosphorus	950	5	14	1	1000	90	5
P+	Boron	1100	5	15	1	900	20	0

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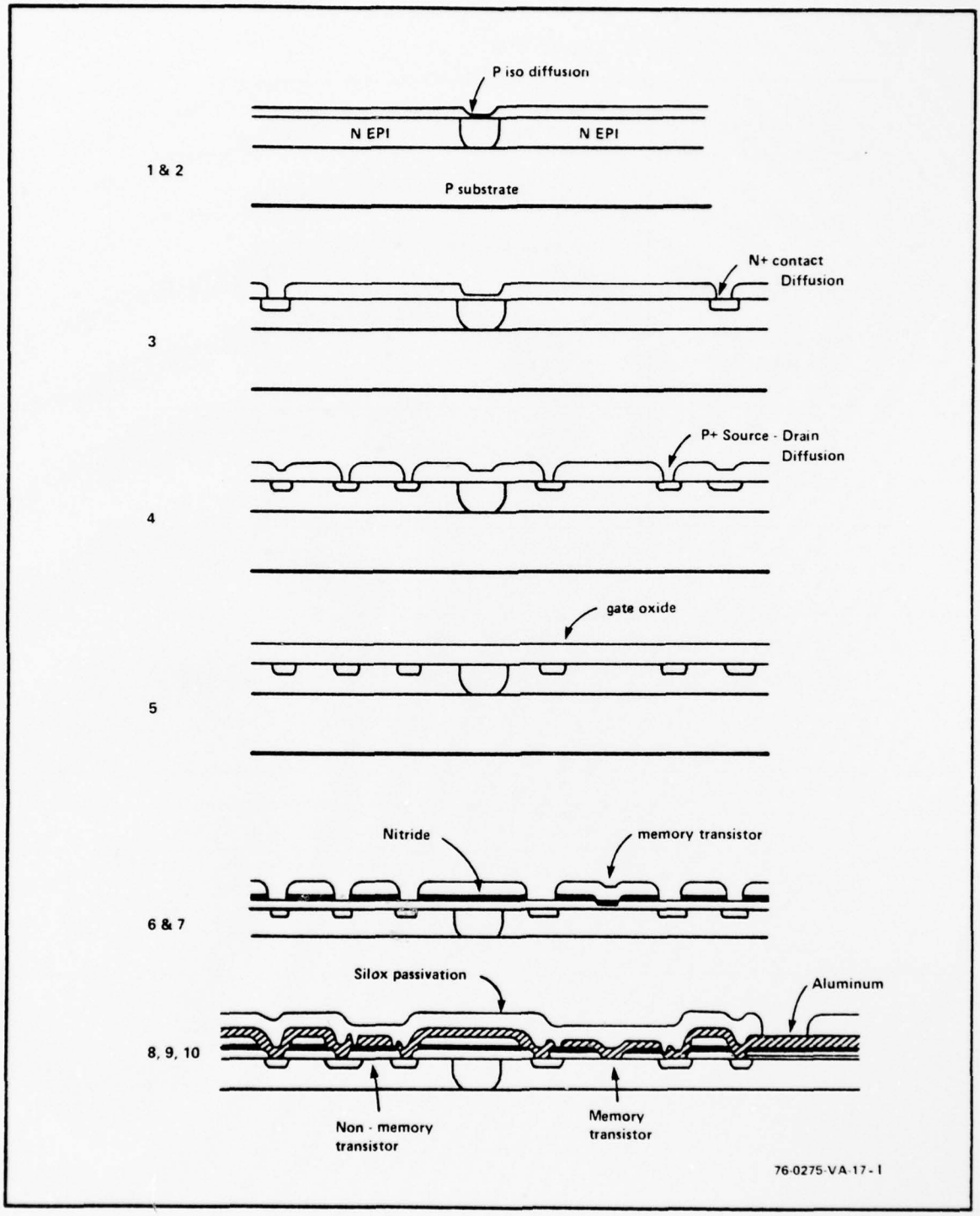

Figure 1-8. Sequential Cross Section of BORAM 6000C

Cycle (7) opens contact windows to silicon by a 2-step etching process. The contact photomask is used to etch through the silox layer. Photoresist is then removed, and the silox layer serves as a mask for the nitride etch. This leaves the gate oxide still in contact windows.

Cycle (8) applies photoresist everywhere except in the gate and contact windows. The contact windows on mask 6 are purposely defined as smaller than the contact windows on mask 5. This forms a stair step structure for metal cross-overs going down to the silicon. An oxide etch is performed which removes the silox over gates and removes the thermal oxide over contacts. Then an aluminum-silicon layer is deposited over the wafer.

Cycle (9) defines the aluminum interconnect pattern, sinters the contacts to silicon, and overcoats the wafer with silox. Finally cycle (10) concludes the sequence by removing the silox overcoat from the bonding pads.

1.2.2 6002 Processing

The proposed BORAM 6002 chip process is identical to the fabrication used for the 6000C except for an additional ion implantation (step 6) which controls inversion in the field regions. This eliminates the use of diffused channel stoppers and helps to reduce the overall size of the chip. Figure 1-9 shows the process sequence.

1.2.3 Nitride Processing

The present system used for deposition of the silicon-nitride layer is an Applied Materials Corporation model AMV1200 reactor shown in figure 1-10. The reactor chamber is shown in figure 1-11. The vertical rotary reactor (VRR) consists of a quartz bell jar that seals to a water cooled base plate. Wafers are processed in a circular susceptor shown in figure 1-12. The susceptor is heated inductively by a profiled RF coil.

As shown in the reactor diagram, reactant gases enter the chamber through the base plate. The gases flow upward and mix with partially reacted gases recirculating in an overall toroidal gas flow pattern. The mixing pattern preheats the incoming gases and lowers reactant super saturation in

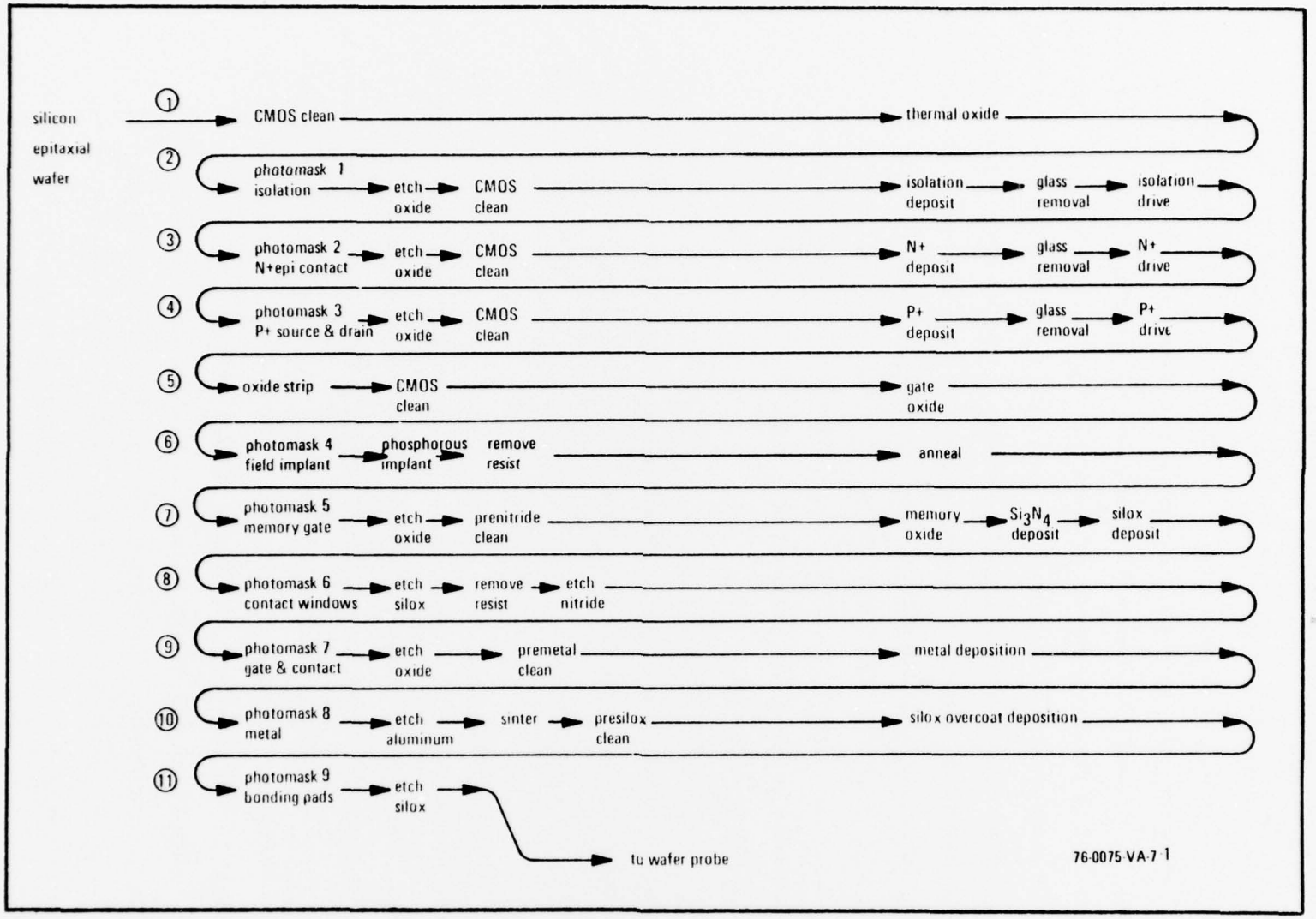

Figure 1-9. BORAM 6002 Fabrication Sequence

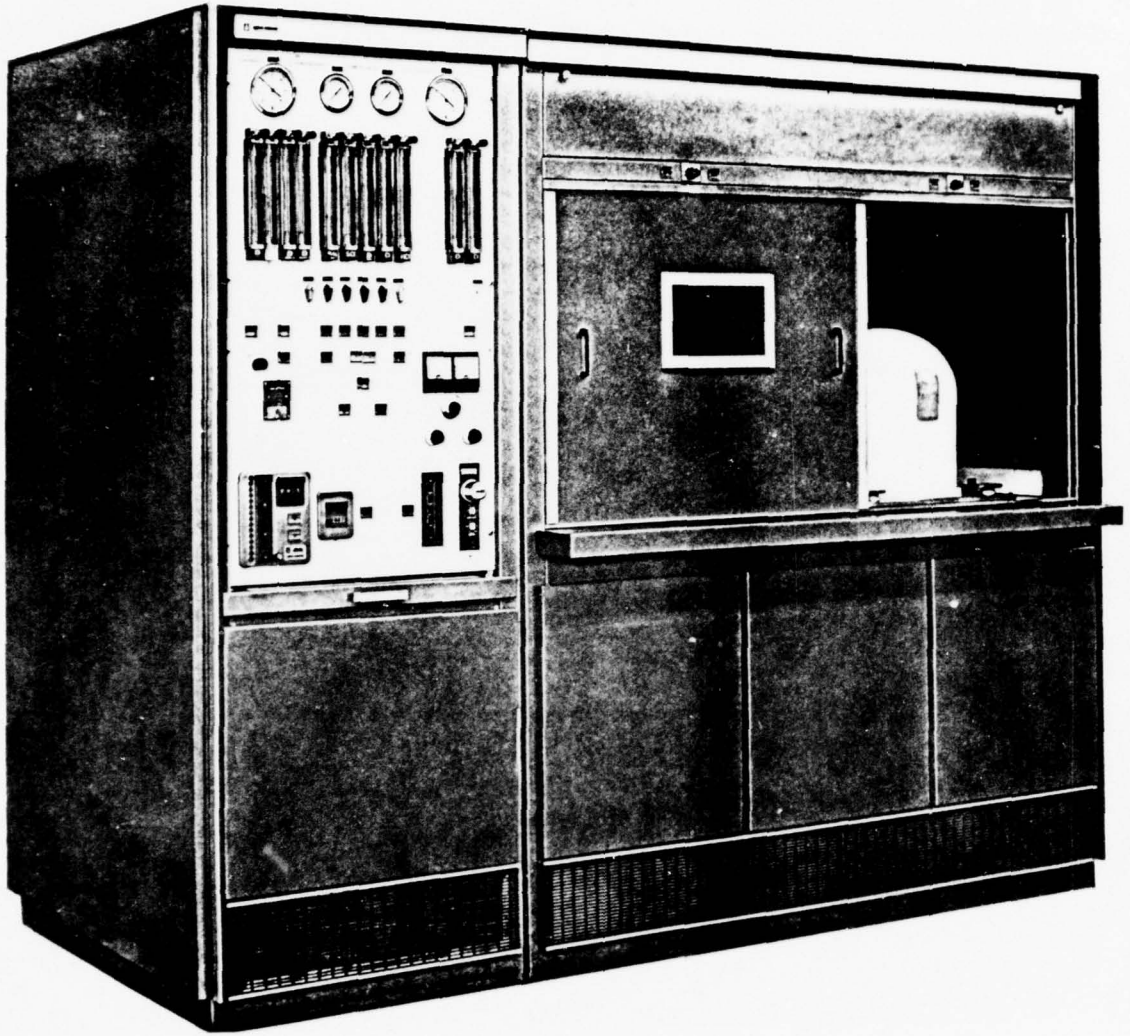

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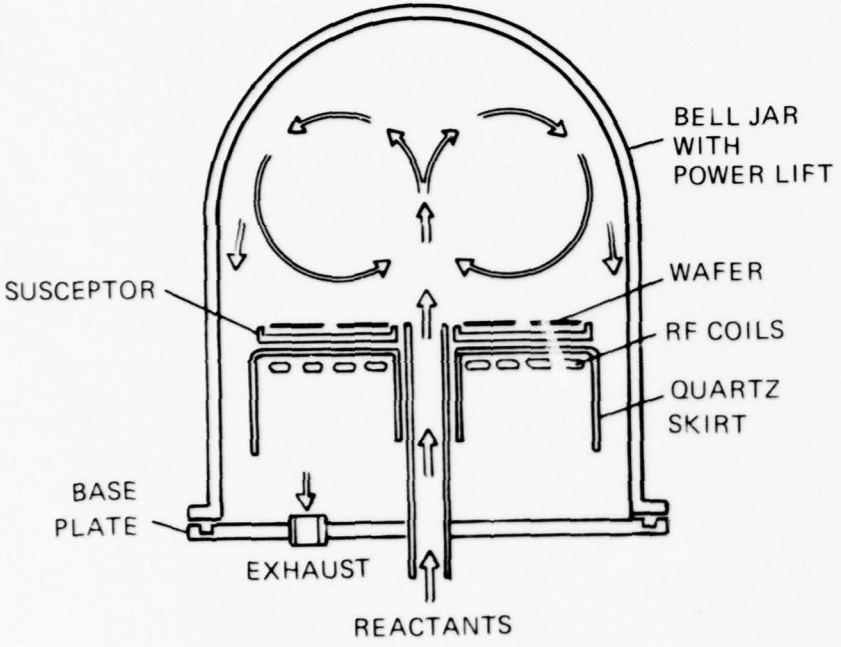
Figure 1-10. Applied Materials Corporation AMV1200 Vertical Rotary Reactor



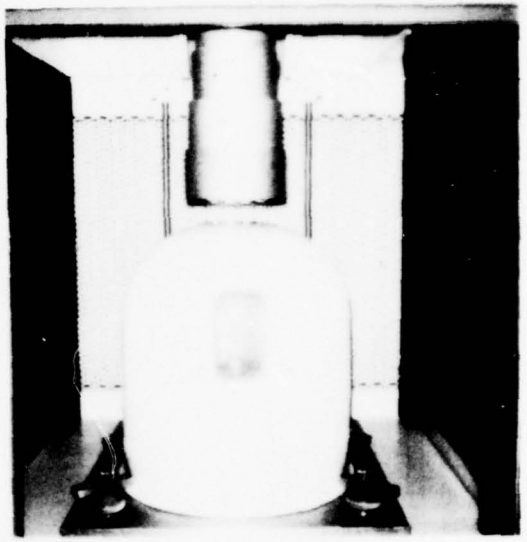


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Figure 1-11. AMV1200 Reactor Bell Jar and Reactor Chamber Diagram

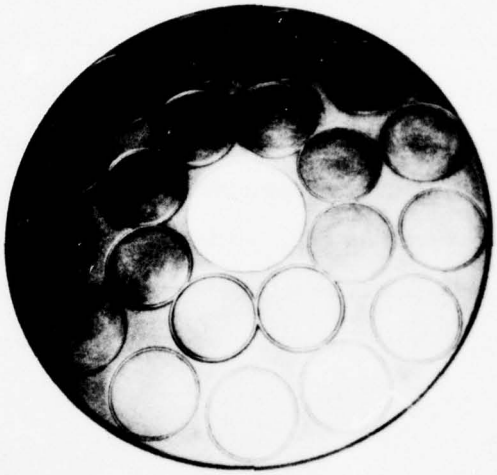

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Figure 1-12. Graphite Susceptor Used for Nitride Deposition

the gas near the wafer surfaces. Film growth takes place in an environment much closer to chemical equilibrium than in horizontal gas flow reactors.

Nitride deposition is the single most critical process in the MNOS BORAM fabrication sequence. As such, it is undergoing a through review. Both the present process and a variety of alternatives are being examined.

Test wafers are used on a daily basis to monitor the quality of the tunneling oxide and nitride composite structure (A nonmemory monitor wafer is also maintained). Three CV plots are prepared for each test capacitor after subjecting the capacitor to a preconditioning pulse sequence.

a. -20 volts 10 sec (saturated write)

b. +20 volts 10 sec (saturated clear)

c. -20 volts 10 sec
+25 volts 100 usec } (pulse clear)

1.3 PROCESS EXPERIMENTS

During this phase of the MM&T project, individual processes are to be examined to improve control and optimize set points for maximum yield. The most critical processes for MNOS BORAM manufacture are the formation of the tunneling oxide and the nitride layer. The results of processing are best revealed in the characteristics of the transistor structures. From the viewpoint of overall LSI circuit processing, the status of the line is best summarized by measurement of final product defect levels.

Progress in optimizing processes during the past quarter has been hampered by nitride deposition equipment problems, and by test equipment problems.

1.3.1 Nitride Control

Nitride processing was disrupted several times during this period by equipment problems. In one case, a faulty mass flow controller on the silane input line gave difficulty. In a separate incident, contamination was encountered in the nitrogen lines. In spite of these problems, a number of experiments were carried out to explore process variation, and to locally optimize set points.

Nitride deposition is believed to be the single most critical process in the MNOS BORAM fabrication sequence. Practical memory arrays operate with fixed external voltages. A change in nitride thickness, therefore, means a change in the initial electrical field across the tunneling oxide. Thin nitride can allow the tunneling layer to be overstressed, and will lead to device degradation. The switching properties of the memory transistor depend on the nature of the tunneling layer and the nitride trap sites. These characteristics are sensitive to nitride processing conditions.

Auger electron spectroscopy and ion beam mass spectroscopy have been used to determine the elemental composition of the MNOS BORAM nitride film and tunneling layer. A variety of samples have been prepared to examine the effects of alternative cleans and process conditions. At the

time of this writing, the data had not been properly organized for presentation. These results will be included in the next quarterly report.

In addition to the above studies, some nitride film samples were sent to Sandia Laboratories for analysis. Dr. Paul Holloway of Sandia coordinated the analysis, and reported the results in a letter as follows: "No contaminants other then C and O were observed, and I believe C is and artifact. The O-level was measured at ~0.3 atom percent..."

Nitride thickness control is a point of some concern. It is desirable to maintain as tight a distribution of thickness variation as the state-of-the-art will allow. Toward this end the limitations of the present nitride process are being documented, ways for improvement of control are being explored, and the merits of alternative processes are being evaluated.

For the MM&T project three measures of thickness dispersion will be computed: the standard deviation, the coefficient of variation, and the range divided by two times the mean. This latter measure is in use by equipment manufacturers, and has been used in the lab because of computational ease.

This last measure requires some comment to clarify its statistical meaning. The lab procedure for judging the uniformity of a sample uses the maximum and minimum thickness measurements.

$$\pm\% \text{ variation} = \left(X_n(\max) - X_n(\min)\right) \Big/ \left(X_n(\max) + X_n(\min)\right)$$

For a sample size of 20 and a normal distribution, the expected value of the ratio of the range R to the universe standard deviation σ is 3.735.

$$\frac{X_n(\max) - X_n(\min)}{X_n(\max) + X_n(\min)} \approx \frac{R_n}{2\overline{X}_n} \approx \frac{3.735\,\sigma_n}{2\overline{X}_n} = 1.8675\,\frac{\sigma_n}{\overline{X}_n}$$

Thickness measurements are performed in the center of each wafer to determine within run uniformity. The vertical rotary reactor (VRR) process was found to exhibit tight control for short periods of time, and then variability begins to increase.

Variation	$\pm R_n/2\bar{X}_n$	$\pm S_n$	$\pm S_n/\bar{X}_n$
within run	±16.5%	±36.5Å	8.5%
run-to-run	±33.2%	±107.0Å	±23.5%

This variability is not seen by the final product because of rework cycles, but it is desirable to avoid rework through tighter control. Several causes of the variability and drift have been identified, and are being studied for possible corrective action.

Individual wafers have been measured on the ellipsometer to determine thickness variations across a wafer. Figure 1-13 shows the results for two particular wafers chosen at random from a nitride run. Wafer A was processed in the outer ring of the susceptor. Wafer B was positioned in the inner ring. Thickness was measured along the wafer diameter perpendicular to the flat. In general, the thickness measured at the center of a wafer tends to be the minimum thickness. Microscopic examination of the wafer surface shows no abrupt features. The thickness variation can sometimes be seen as a slight difference in color.

Table 1-5 shows the thickness readings obtained for one particular VRR deposition. This run was performed using a new susceptor. It is characteristic that variability will increase as a susceptor ages. This is believed

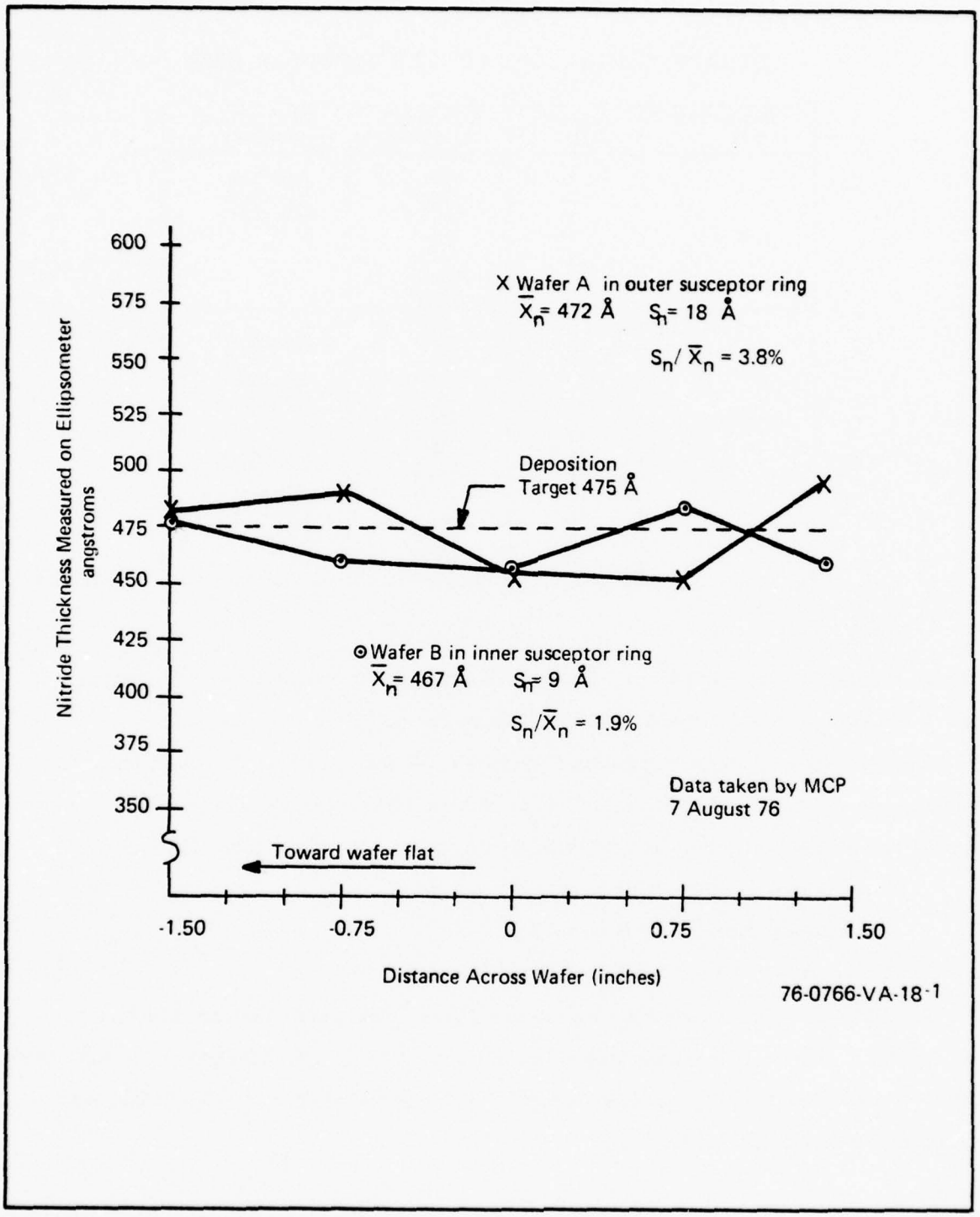

Figure 1-13. Nitride Thickness Variation

TABLE 1-5

NITRIDE THICKNESS FOR VRR MONITOR RUN

SUSCEPTOR RING	WAFER SLOT	THICKNESS (ANGSTROMS)	STATISTICAL SUMMARY
INNER	1	420.8	Inner Ring
	2	380.6	$\bar{X}_n = 397.6$
	3	397.8	$S_n = 12.4$
	4	392.0	$S_n/\bar{X}_n = 3.1\%$
	5	394.9	
	6	393.4	
	7	403.7	
OUTER	8	443.6	
	9	426.6	Outer Ring
	10	411.1	$\bar{X}_n = 403.3$
	11	402.1	$S_n = 20.4$
	12	393.7	$S_n/\bar{X}_n = 5.1\%$
	13	403.6	
	14	380.2	
	15	377.4	Entire Susceptor
	16	376.0	$\bar{X}_n = 401.4$
	17	415.0	$S_n = 18.0$
	18	377.3	$S_n/\bar{X}_n = 4.5\%$
	19	407.8	
	20	415.7	
	21	416.0	

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to be a function of emissivity and/or changes in thermal characteristics as the susceptor accumulates a nitride coating.

An alternate nitride deposition process shows promise of much improved thickness control. Vendors of low pressure chemical vapor deposition systems (LPCVD) are claiming typical uniformity specifications of:

- within a wafer ±5% to ±3%
- within a run ±5% to ±2%
- run-to-run ±5% to ±2%

An LPCVD system involves a conventional diffusion tube arrangement with about 100 to 200 wafers in a ladder type boat. Manufacturers claim less than 2 pinholes for a 3-inch wafer, index of refraction of 2.00 ±0.02, and reduced operating costs.

Currently, LPCVD systems are being evaluated for procurement and use in the MNOS BORAM pilot line. Individual wafers have been prepared using the VRR and LPCVD systems to compare uniformity. Table 1-6 shows a typical result for a nominal 960-angstrom film. The thickness variation of the LPCVD sample is less than 27 percent of that for the VRR sample. The measurements were taken at five equally spaced points on a diameter of the 3-inch wafers.

Other LPCVD wafer evaluations have confirmed that capacitors exhibit adequate, and uniform saturated and pulsed memory threshold levels. Currently, BORAM 6000C devices are being fabricated to further explore the capabilities of this process.

Threshold voltage windows and pulse response are another dimension of product performance which is sensitive to nitride processing conditions. Several experiments have been performed on the VRR to locally optimize process set points for improvement of response characteristics. The results of these investigations were clouded by variability in response associated with the VRR equipment problems mentioned previously. Figure 1-14 shows the results of a search for the best deposition rate for a specific set of process conditions. Experiments of this nature will be continuing during the next quarter.

1.3.2 Nonmemory Transistors

The nonmemory transistor structure depends on the quality of the thermal oxide and the nitride layer. The gate oxide process is monitored daily by processing and performing CV measurements on two wafers. The observed threshold voltages for the past quarter appear in figure 1-15. Monitor results serve as an alarm to the product and process engineers that corrective action is needed.

Nitride deposition runs are also monitored for nonmemory transistor characteristics. Figure 1-16 provides a graph of nonmemory threshold voltage in a format similar to that for the oxide monitor.

TABLE 1-6

WITHIN WAFER NITRIDE VARIABILITY FOR LPCVD SAMPLE AND A VERTICAL ROTARY REACTOR SAMPLE

MEASUREMENT POINT OR STATISTIC	LPCVD SAMPLE		VRR SAMPLE	
	THICKNESS (ANGSTROMS)	INDEX OF REFRACTION (NUMERIC)	THICKNESS (ANGSTROMS)	INDEX OF REFRACTION (NUMERIC)
1	956	2.02	1025.6	1.95
2	947	2.03	981.9	1.96
3	954	2.02	963.0	1.96
4	972	1.99	944.0	1.96
5	974	2.01	907.5	1.96
$\bar{X}_n$	960.60	2.014	964.40	1.958
S_n	11.82	0.015	43.90	0.004
$3S_n$	35.47	0.046	131.69	0.013
$S_n/\bar{X}_n$	1.23%	0.71%	4.55%	0.228%
$3S_n/\bar{X}_n$	3.69%	2.13%	13.65%	0.685%
$\frac{X_n(max) - X_n(min)}{X_n(max) + X_n(min)}$	1.41%	0.995%	6.11%	0.256%

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1.3.3 Memory Transistors

To properly examine the performance of a memory transistor, it is necessary to consider several different parameters. For MNOS BORAM, the major parameters that are monitored are V_{HC} (saturated), V_{HC} (pulsed), V_{LC} (saturated), V_{LC} (pulsed), and retention slopes. These parameters are to be observed as a function of erase write cycles out to 10^{10} accumulated cycles. In addition, the pulse response curves for writting and clearing using various pulse widths are to be monitored.

The primary tool for measuring these characteristics is a special test unit called the "VT tester". At present, the VT tester is in the final debugging stages, and needs some circuit revision. Personnel workload schedule conflicts have delayed that effort. It is expected that the next quarterly report will contain test results to document the accuracy and precision of the VT tester.

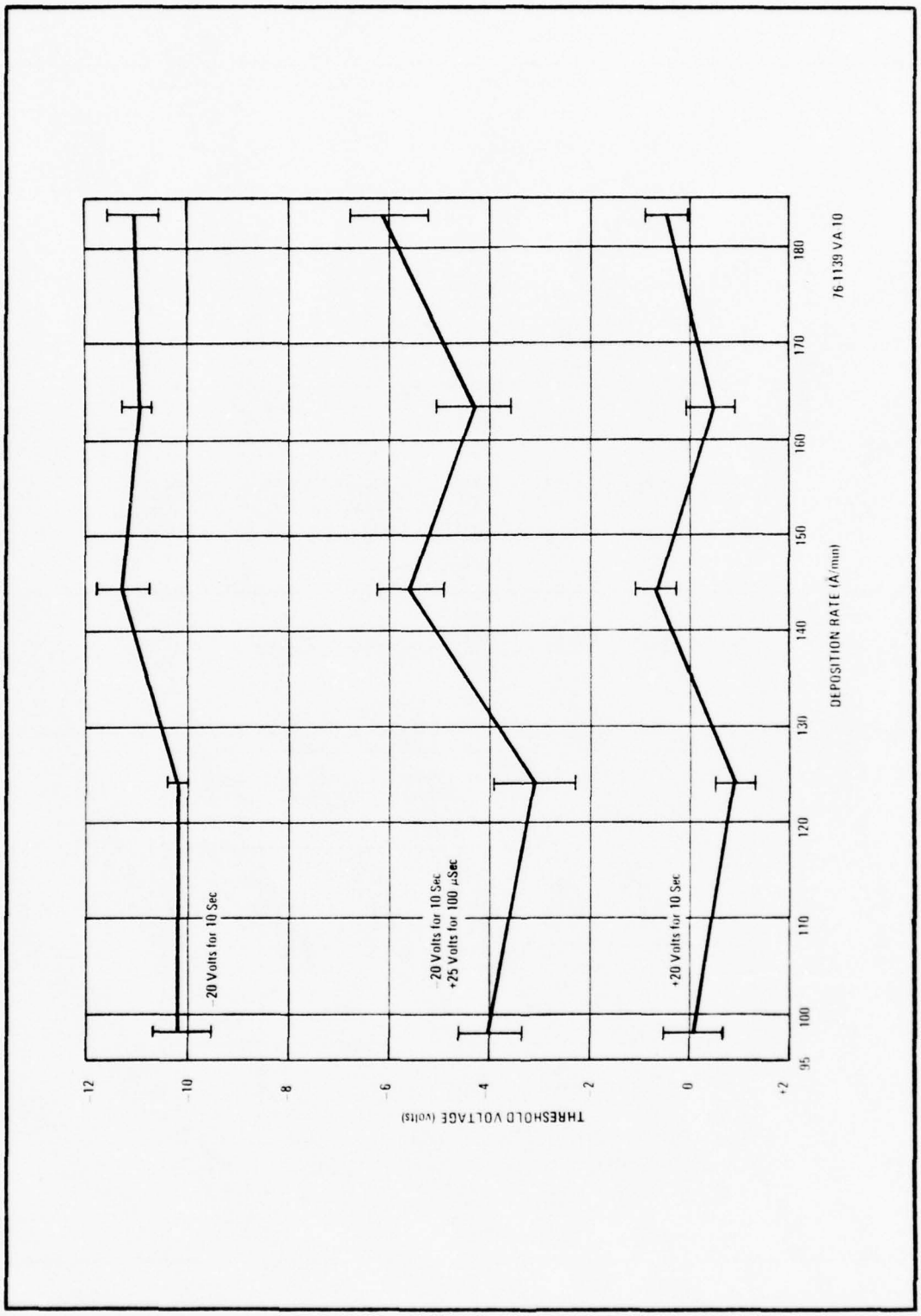

Figure 1-14. Deposition Rate vs DC and Pulse Response

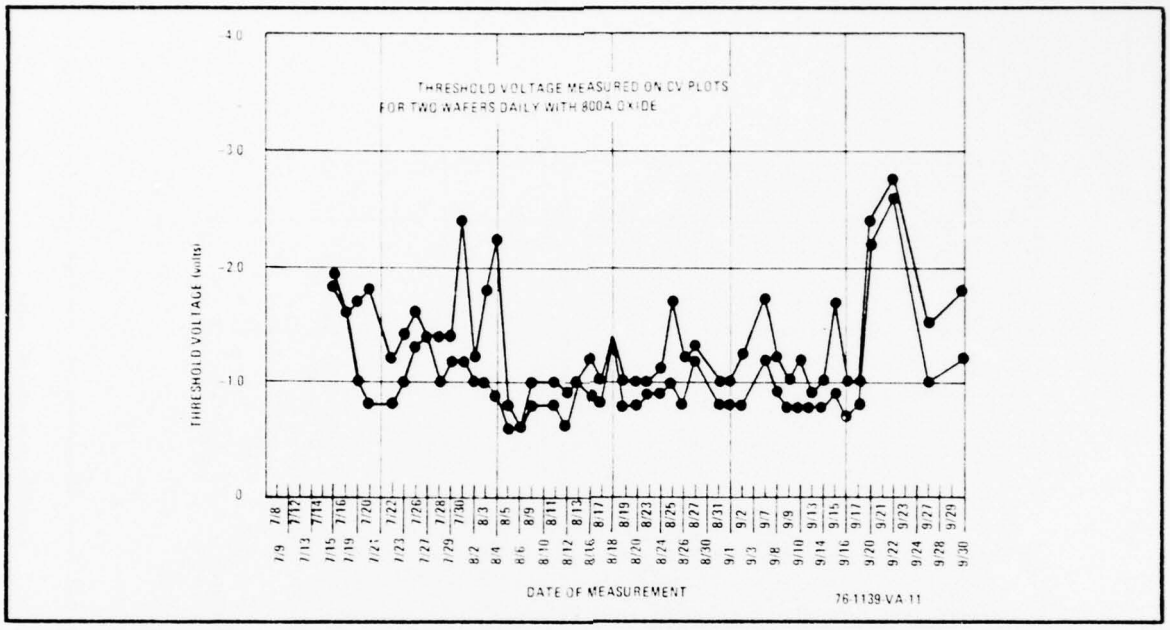

Figure 1-15. Gate Oxide Quality Monitor

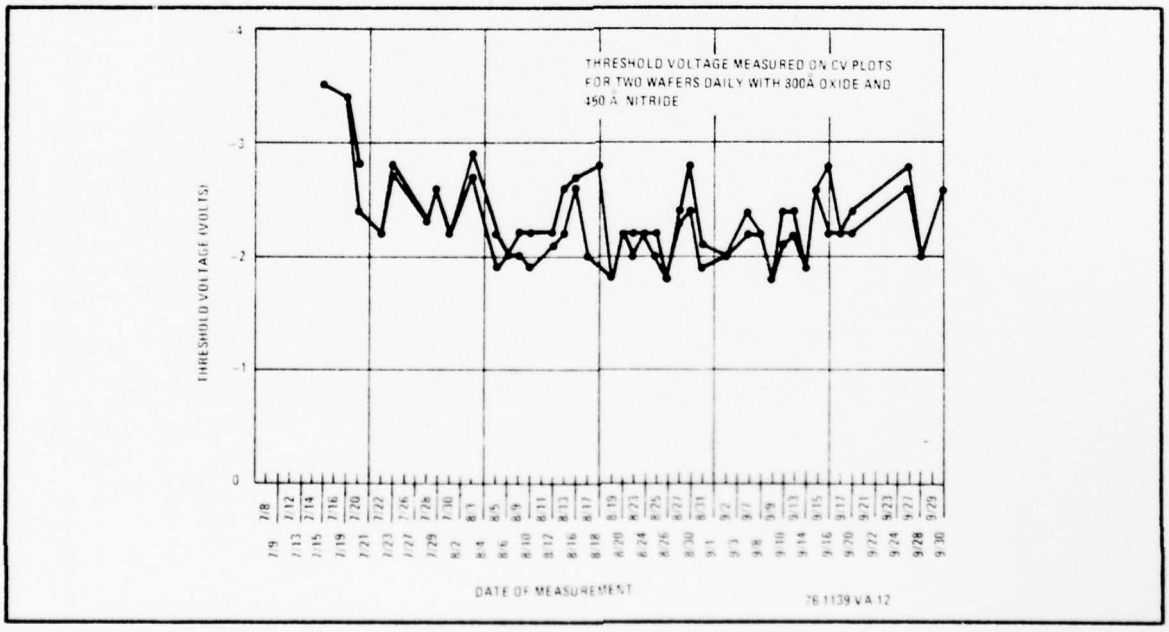

Figure 1-16. MNOS Transistor Nonmemory Threshold Monitor

Activity during this quarter has been oriented toward establishing the capability and procedures for routine collection of information on memory transistor performance. Present concepts of the BORAM pilot line call for feedback of performance data from three major sources.

The earliest point of data collection is derived from the CV tests performed on monitor wafers after nitride deposition. CV monitors have proven to be a sensitive indicator of process problems. The recent bout of VRR equipment difficulities was reflected in the magnitude of the pulsed clear threshold voltage observed on the monitors. Figure 1-17 shows the recovery of the clear level when corrective actions were completed on 10 October 1976.

The second source of memory transistor performance data is the wafer probe test on the Macrodata 154 system. Each BORAM die contains a discrete memory transistor. The threshold voltage at 10 microamperes for that transistor will be observed and recorded for 3 different pulse conditions:

a. +25 volts, 200 μsec

b. -25 volts, 10 μsec

c. +25 volts, 200 μsec; -25 volts, 100 μsec

As discussed previously, the third source of memory transistor data is the VT tester. After wafer probe, sample devices will be packaged for detailed analysis. The packaged parts will be retested on the Macrodata 154, and then pulse response and retention slope data will be obtained from the VT tester. Individual samples will then follow a specific test plan. Some devices will be subjected to erase write cycle stress with periodic retest. Some parts will be reserved for long term retention checks. Other parts will be placed under various accelerated stress conditions to examine retention properties and device failure rate.

1.3.4 Defect Level Investigations

A series of studies are underway to measure defect densities related to yield at wafer probe. The data from these studies will be use to focus

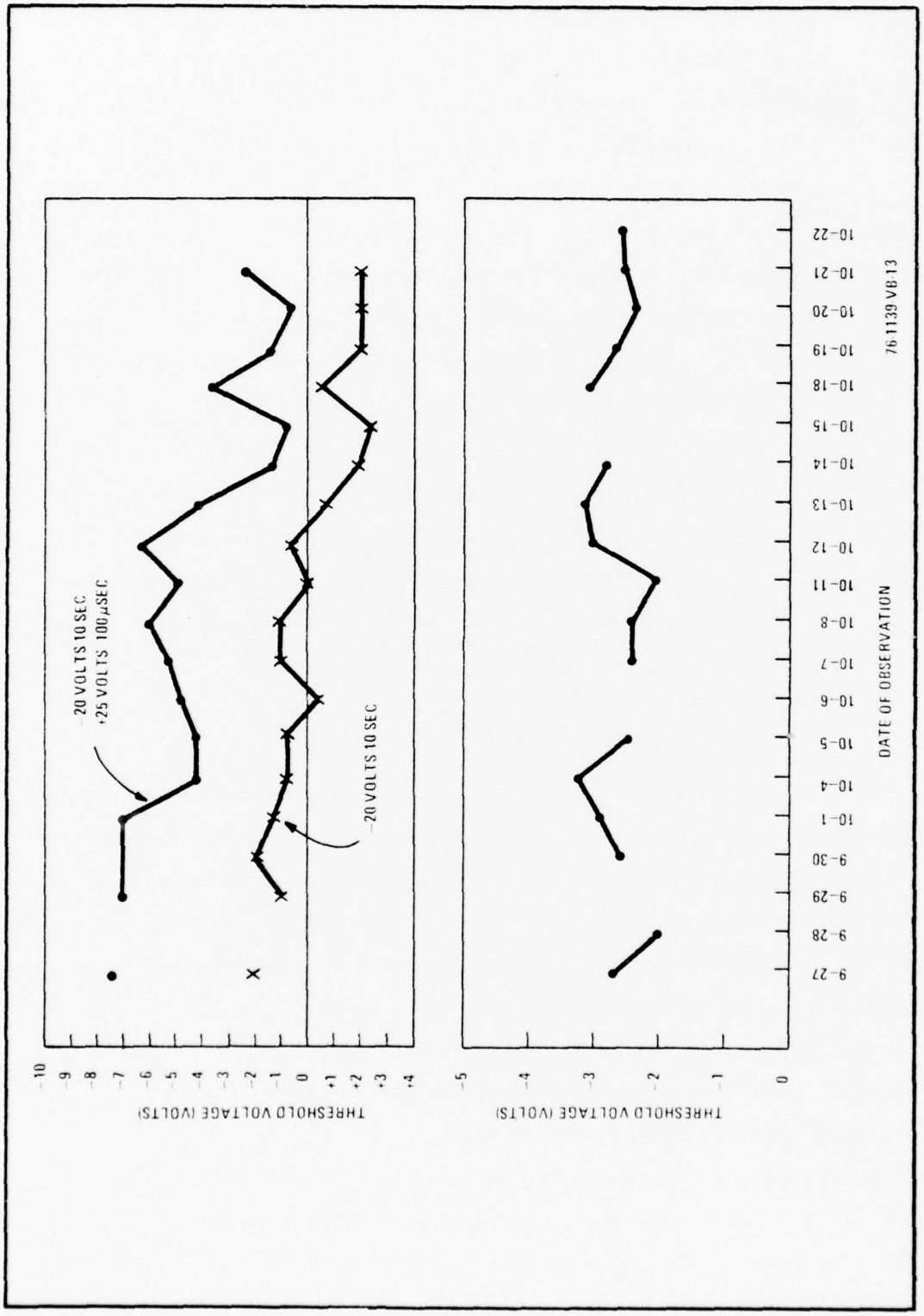

Figure 1-17. BORAM Nitride Monitor Results

engineering effort where the largest economic return may be obtained. In addition, the data will be used to validate and/or modify the mathematical yield model used for BORAM cost projections.

The defect density of final product is being measured at probe test. The logic of the test program identifies and tabulates chips with an operating shift register, 1K of memory, and 2K of memory functional. The die area for each of these circuits is known, and the yield for each circuit can be calculated from the tabulated pass fail counts. Assuming Bose-Einstein statistics and a common effective defect density for all circuits on the wafer, a computer data reduction program can provide a defect density estimate.

The report generation computer program is currently being prepared. The plan is to provide the defect density and yield information for each wafer, and for each lot. Lot summary numbers will be saved in a master file for line trend analysis.

The primary tool for gathering defect density information for specific aspects of the fabrication sequence is visual inspection. As a starting point, a sampling plan has been established for inspection of photomask working plates for the 6000C chip.

Eight masks out of every box of 30 plates are being examined under 100X. The 38-die positions in the central portion of the mask are being inspected, and defect counts are recorded on a wafer map.

At a later date this effort will be extended to other areas of mask making, and to product in the line. Inspections will be repeated to determine the impact of process changes.

1.4 PRODUCTION ACTIVITY

Activities for this first quarter of the MM&T Project were directed at establishing schedules and milestones, assigning personnel responsibilities, creating the product documentation package, initiating the production and engineering information systems, allocating equipment, setting up processes and test programs, and initiating production runs. First processing lots were completed and testing started during this period.

1.4.1 Engineering Sample Fabrication

A production plan to satisfy requirements for Engineering Sample 1 and 2 was formulated as one of the first items after contract award. Key aspects of the plan involve wafer starts, daily process cycles, wafers completed, and chips completed. These items are displayed in table 1-7 which shows the planned versus actual quantities as of the quarter ending date. The deficits from plan to actual in the "process cycles" and "wafers completed" categories are due to silicon-nitride deposition equipment problems which resulted in a "hold" on wafer lots prior to that step in the process. As the "comments" column indicates, a significant inventory of wafers has accumulated at this step. Table 1-8 shows the in-line inventory status. As of this writing, the equipment problems have been eliminated and process control reestablished which will allow a resumption of work in October. A make-up schedule will be established in order to meet original schedule milestones.

1.4.2 Process Monitoring

In order to determine critical process reproducibility control charts have been instituted. These charts are intended to supply long term process variability information as well as to indicate localized "out-of-control" conditions. The charts are maintained by Quality Control personnel and are

reviewed regularly by Quality Control Engineering and MM&T project engineers. The processes currently monitored are as follows:

a. Isolation Deposit - ρ_s
b. Isolation Drive - ρ_s, X_j
c. N+ Deposition - ρ_s
d. N+ Drive - ρ_s, X_j
e. P+ Deposition - ρ_s
f. P+ Drive - ρ_s, X_j
g. Date oxidation - t_o
h. Si_3N_4 - t_o, I.R.
i. Metallization - t

In addition to these charts, project engineering personnel are accumulating data regarding processes under investigation for manfacturability improvement. These involve primarily those processes associated with the formation of the nonmemory and memory transistor characteristics.

1.4.3 Process Experimentation

All significant experimentation for the period has been directed at identifying and controlling the process variables which affect the characteristics and reproducibility of the memory gate structure. Data has been collected on several approaches to the formation of this structure. Sufficient data for selection of a best approach has not yet been gathered. The primary areas under investigation were summarized in paragraph 1.3.1 above.

TABLE 1-7

STATUS OF BORAM ENGINEERING SAMPLE 1 PRODUCTION

Event	Plan	Actual	Comments
Avg. Daily Starts	3	3.5	
Cum Daily Starts thru 9/30/76	180	212	
Avg. Daily Process Cycles	20	14	
Cum Process Cycles thru 9/30/76	1000	712	As of 10/12/76, 105 wafers are inv at SiN dep.
Avg. Daily Wafers Completed	2	0.725	
Cum Wafers Completed 9/30/76	78	29	Hold at SiN Dep. prevented completing wafers
Cum Chips Wafer Probe 9/30/76	370	0	76 Complete as of 10/12/76

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TABLE 1-8

INVENTORY STATUS (9/30/76)

Station	Code	Quantity	% of Process Complete
Epi/Laser	120	10	0
N+ Photo	151	15	20
Phos Dep	160	13	25
Mem Photo	191	9	43
SiN Dep	200	84	50
Test	271	29	93

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2. CONCLUSIONS

The MNOS BORAM manufacturing methods project is progressing according to plan. Engineering objectives are being achieved. Equipment problems and electrical test delays have caused an approximate three week schedule slippage.

The production line has been defined and manufacturing documentation has been reviewed. Process controls have been reviewed and refined. Process variability is currently being characterized, and actions to achieve improvements are being studied.

The most negative occurence during the quarter was a series of equipment problems with the vertical nitride reactor. These items have been corrected. The most positive result for the quarter was the success in shrinking the BORAM die. The very small BORAM 6002 chip is expected to cut die cost by a factor of five.

3. PROGRAM FOR NEXT INTERVAL

A revised production schedule for Engineering Samples 1 and 2 has been generated to make up for deficits accumulated due to the equipment problems encountered at nitride deposition.

Statically significant data for characteristics such as refractive index, conductivity, thickness, pulse response, retentivity, and endurance will be accumulated for the alternative memory gate processes as well as for the present standard process.

Refinement of the wafer test program to better characterize and test for memory characteristics (retention, uniformity, etc.) will be a primary objective during the next period as well as implementation of the "V_T Tester" to measure the longer term nature of these parameters.

Work will begin on a modification of the Westinghouse "Oracle" computer model to represent the 6000C product flow. During the next period, the inputs necessary to construct the model (time values, queues, etc.) will be determined. The "Oracle" program will be revised, and the first computer run will be generated.

4. PUBLICATIONS, REPORTS, AND MEETINGS

On 12 August 1976, the MNOS BORAM manufacturing methods and technology project post-award conference was held at the Westinghouse Advanced Technology Laboratories in Elkridge, Maryland. The attendees included:

E. Ahlstrom	ECOM	D. Hadden	ECOM
D. Biser	ECOM	W. Hendrix	AFPRO
J. Brewer	Westinghouse	J. Hetrick	Westinghouse
G. Cooley	Westinghouse	H. Mette	ECOM
R. Conquest	Westinghouse	L. Palkuti	NRL
J. Dzimianski	Westinghouse	F. Phillips	NATC
R. Fedorak	NADC	G. Poward	Westinghouse
D. Fischer	Westinghouse	G. Shapiro	Westinghouse
E. Gallagher	ECOM	G. Strull	Westinghouse
B. Haas	Westinghouse	H. Weinstein	Westinghouse

The morning session featured an overall review of the project objectives of developing a high volume production capability for low cost MNOS BORAM hybrid circuits. The importance of the program to the military and to the future of the MNOS technology was stressed. A successful pilot run would signal the readiness of the technology for widespread usage. The presentation of manufacturing plans was followed by a plant tour.

The afternoon session was devoted to a detailed technical review of improvements planned for the BORAM chip and the hybrid circuit. The session concluded with an action item summary by the ACO, Mr. Warren Hendrix.

During the past quarter, there were no publications or reports derived directly from this MM&T project.

5. IDENTIFICATION OF TECHNICIANS

Figure 5-1 describes the Westinghouse organizational structure for the MNOS BORAM MM&T project. Resumes of those individuals making technical contributions to the program appear below.

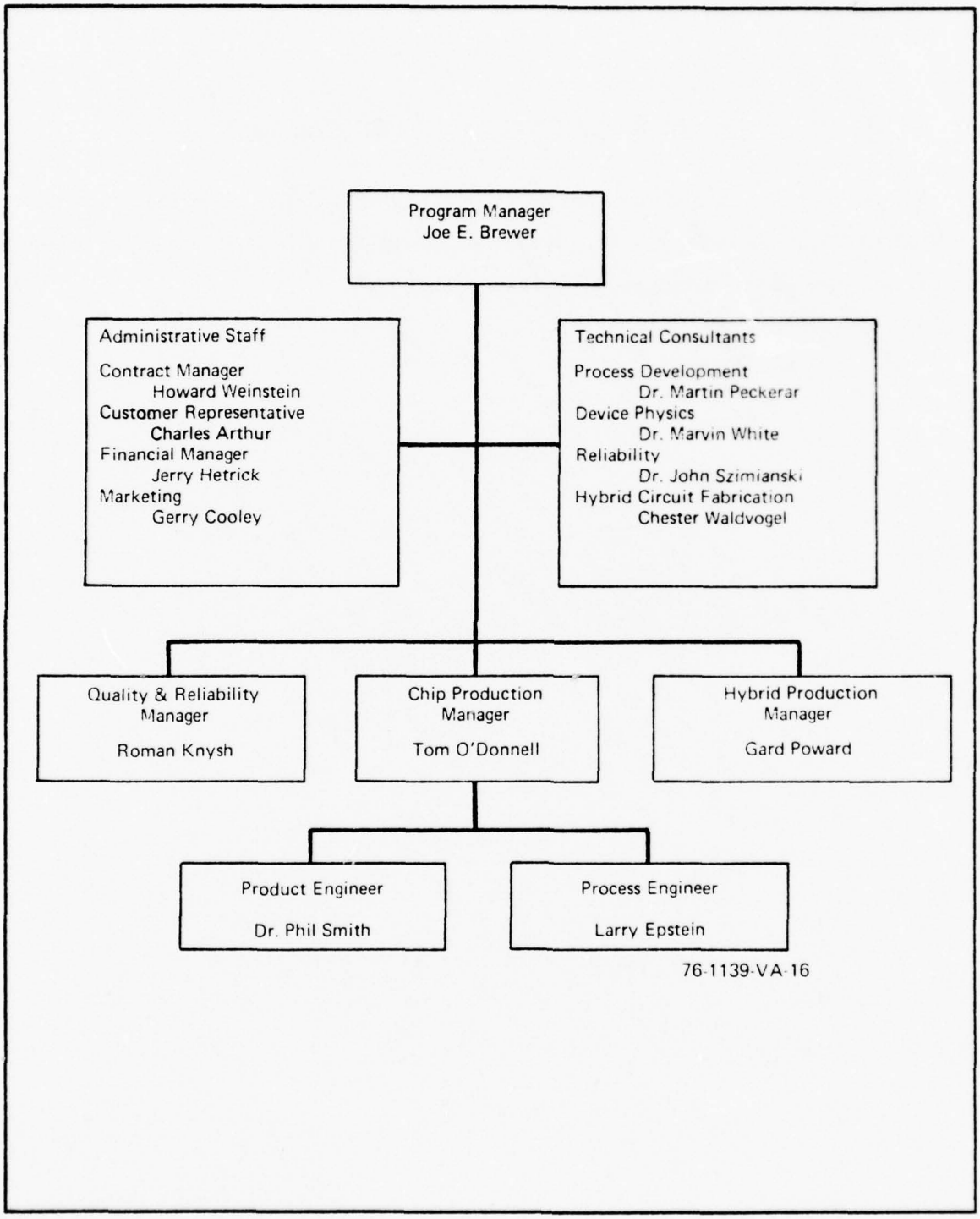

Figure 5-1. Westinghouse MNOS BORAM Program Organization

NAME: Joe E. Brewer, Advisory Engineer

EDUCATION: BSEE° Milwaukee School of Engineering, 1961
Graduate work in mathematics, University of Wisconsin

EXPERIENCE: Westinghouse Electric Corporation

1976 - Present System Development Division, Computing and Data Systems Department, MNOS BORAM Program Manager

1970 - 1976 Command and Control Division, Electronic Systems Department, Hardware and software development for weapon systems with emphasis computer and memory systems. On assignment as Manager of BORAM nonvolatile semiconductor secondary memory system development.

1969 - 1970 Underseas Division, Weapons Department. Fellow Engineer responsible for advanced development of computers, memory systems, signal processors, and SONAR.

1966 - 1969 Molecular Electronics Division, Manufacturing Department. Supervisor of Product Engineering for Custom Products Line. Responsible for design, development and manufacture of monolithic integrated circuits for high reliability applications (Titan III and Minuteman).

Centralab Division Globe Union Incorporated

1964 - 1966 Product Development Department Manager of Advanced Design Section responsible for new product design with emphasis on hybrid integrated circuits. Introduced the use of computer aided techniques as a primary tool for the 12-man design team.

NAME: Joe E. Brewer (Continued)

EXPERIENCE: (Continued)

1963 - 1964	Engineering Services Department Engineer I consultant and project engineer for product design and analysis. Operated a technical computing service for engineering and research groups.
1961 - 1963	Engineering Services Department Engineer II performed circuit design and automatic test equipment design.
1958 - 1961	Manufacturing Engineering Department Technician on the packaged electronic circuit product line.

PATENTS: #3590345 - Double Wall PN Junction Isolation Technique
#3815124 - Envelope and Waveform A/D Converter
1 pending - Addressable Clear for MNOS Memory Arrays.
10 disclosures.

PUBLICATIONS: "Hybrid Circuit Design with ECAP", University of Wisconsin Engineering Institute, April 1966, Madison, Wisconsin.

"The Circuit Manufacturer and Computer Aided Reliability Analysis", University of Wisconsin Engineering Institute, January 1967, Milwaukee, Wisconsin.

"An Underwater System Director: LOGPRO#3", IEEE OCEAN 72 Conference, September 1972, Newport, Rhode Island.

"A Torpedo System Director: LOGPRO#3", GOMAC Conference, October 1972, San Diego, California.

"A BORAM System for the U.S. Army", AFAL MNOS Workshop, March 1973, WPAFB Dayton, Ohio.

"Nonvolatile Block Oriented Random Access Memory", IEEE Solid State Circuits Conference, February 1974, Philadelphia, Pennsylvania.

NAME: Joe E. Brewer (Continued)

PUBLICATIONS: (Continued)

"Block Oriented Random Access MNOS Memory", National Computer Conference, May 1974, Chicago, Illinois.

"MNOS Secondary Storage", NAECON Conference, May 1974, Dayton, Ohio.

"MNOS: A Novolatile Semiconductor Storage", IEEE International Magnetics Conference, May 1974, Toronto, Canada.

"MNOS Density Parameters" IEEE NVSM Workshop, August 1976, Vail, Colorado.

"Army/Navy MNOS BORAM", GOMAC Conference, November, 1976, Lake Buena Vista, Florida.

SOCIETIES:

IEEE Senior Member
Technical Committee on Computer Architecture
Technical Committee on Mass Storage
ACM, SIGARCH, SIGMICRO, SIGART

NAME: M.C. Peckerar, Senior Engineer, Process Development

EDUCATION: B.S., Physics, SUNY at StonyBrook, 1968.
M.S., Physics, 1971
Ph.D., Engineering Materials, University of Maryland, 1976

EXPERIENCE:

1968 - 1974 NASA/Goddard Space Flight Center, Physicist, reliability of semiconductor devices, specialization in area of surface studies.

1974 - 1976 Naval Research Laboratory, Washington, D.C., Research Physicist, working in the areas of X-ray analysis of materials (diffraction, flourescence XPS, etc), X-ray imaging and detection techniques.

1976 - Present Westinghouse Electric Corporation, Senior Engineer responsible for process development, control and analysis. Present work includes the study of dual dielectric formations and interface charging control.

PUBLICATIONS: Government Publications - "Semiconductor Metallization Studies," NASA/GSFC FMR 10-003, January 1971 (with R.J. Anstead and S. Floyd).

"A Study of the Electrical and Thermal Characteristics of Fusewire," NASA/GSFC FMR 04-001, July 1970 (with E. Thomas).

Papers - "Failure Analysis with the Electron Mecroprobe," presented at the Combined Area IEEE Electron Device and Parts Materials and Packaging Group Meeting, March 1972.

"Electron Beam Studies of Schottky Barrier Detector Surfaces," IEEE Trans. Nuc. Sci NS-20, 383 (1973).

"Measurement and Calculation of Absolute Intensities of X-Ray Spectra," J. Appl. Phys. 46, 4537 (1975) (with D.B. Brown and J.V. Gilfrich).

"On the Origin of the Increase in Schottky Barrier Height with Increasing Interfacial Oxide Thickness°" J. Appl. Phys. 45, 4652 (1974).

NAME: M.C. Peckerar (Continued)

PUBLICATIONS: (Continued)

"Open Circuit Voltage of MIS Schottky Diode Solar Cells," Proc. IEEE IEDM, 213 (1975) (with H.C. Lin and R.W. Kocher).

"X-Ray Imaging with Charge-Coupled Devices," Bulletin of the American Physical Society, 21, 597 (1976) (with D. Baker and D.J. Nagel).

"The Role of Electron Trapping in the Plasma Anodization of Aluminum," Journal of the Electrochemical Society, 123, 190C (1976) (with S. Mak).

"Influence of Electric Field Strength and Oxide Composition on Charge Retentivity and Endurance of Thin-Oxide, Non-volatile MNOS Memory Transistors," Accepted for publication in Proceedings of 1976 IEDM (with M.H. White and J. Dzimianski).

"Ion Implanted Schottky Solar Cells," accepted for publication in Proceedings of 1976 IEDM (with P. Pai, H.C. Lin, and R. Kocher).

SOCIETIES: American Physical Society, Electrochemical Society

NAME: Marvin H. White, Advisory Engineer

EDUCATION: A.S. in Engineering, Henry Ford Community College, 1955 - 1957
B.S.E. Physics and B.S.E. Mathematics, University of Michigan Engineering College, 1957 - 1960
M.S. Physics, University of Michigan, Horace Rackham Graduate School, 1960 - 1961
Ph. D.E.E., Ohio State University, Graduate School, 1966 - 1969
Dissertation: Characterization of Microwave Transistors - Advisor: Marlin O. Thurston

EXPERIENCE:

1959 - 1960	Research Assistant - University of Michigan, Optical Properties of Semiconductors.
1961 - 1962	Westinghouse Electric Corporation - Graduate Student Program - Assignments in Solid State Devices.
1962 - 1964	Project Engineer on contracts calling for research and development of infrared camera tubes and IR Mosaic P-N Junction sensing layers. Vidicon Characterization Silicon Diode. High frequency transistor amplifiers and solid-state control grid devices. Investigation of Si-SiO_2 interface with C-V measurements.
1964 - 1965	Project Engineer on contracts calling for the analysis and development of bistable multivibrator circuits using MOS devices. Design and development of N and P channel. Complementary MOS Transistors and CMOS Circuits.
1965 - 1966	Project Engineer on contract calling for the design and development of MOS and CMOS circuits. Surface characteristics of CMOS structures. Breadboarding of standard component semiconductor circuits and the translation of those circuits to integrated circuit form. Responsible for the organization of integrated circuit courses the design and fabrication of integrated circuits.

NAME: Marvin H. White, (Continued)

EXPERIENCE: (Continued)

1966 - 1968	Instructor - Ohio State University, courses pertaining to solid state electronics for under-graduates.
1968 - 1969	Westinghouse Electric Corporation - Senior Engineer - responsible for the analysis, design and development of low power, microwave bipolar transistors for L and S band amplification.
1969 - 1970	Fellow Engineer - responsible for analysis and development of microwave solid state devices. Study of semiconductor surfaces for maintenance of process control in MOS circuit development. Consultant on all electronic fuze program for the analysis, design and development of sensors and associated signal processing in integrated circuit form.
1970 - 1971	Investigation of charge transport and storage in multiple dielectric films (MNOS and MAOS) for non-volatile semiconductor memories. Study of Si-SiO_2 interface with c-t, quasi-static and noise measurements. Responsible for the design and development of high power, pulsed, microwave transistor amplifiers for L and S band.
1971 - 1972	Analysis, design, development and evaluation of CCD and photodiode line and area imaging arrays. Analysis of factors which effect the noise in sensor arrays.
1972 - Present	Advisory Engineer - analysis and design of surface and buried channel CCD and MNOS devices for signal processing and memories. Evaluation of electro-optical parametersin imaging arrays.
1962 - 1966	Instructor in Westinghouse School of Applied Engineering Science.

NAME: Marvin H. White (Continued)

EXPERIENCE: (Continued) 1966 - Present Courses in Applied Transistor Electronics and Semiconductor Devices.

PATENTS: 10 awarded, 7 pending.

PUBLICATIONS: "Complementary MOS Transistors", M.H. White and J.R. Cricchi, Solid State Electronics, 9, pg. 991-1008, October, 1966.

"Large Scale Complementary MOS Transistor Arrays", J.R. Cricchi and M.H. White, International Electron Device Meeting, Washington, D.C., October, 1966.

"A Voltage-Controlled MOS-FET Integrator", M.H. White, Proceeding of the IEEE (Correspondence), 54, pg. 421-422, March, 1966.

"Metal-Oxide-Semiconductor (MOS) Small Signal Equivalent Circuit", M.H. White and R.C. Gallagher, Proceedings of the IEEE (Correspondence) 53, pg. 314-315, March, 1965.

"Electric Fields in Transistors", Vasil Uzunoglu and M.H. White, Semiconductor Products and Solid State Technology, February, 1965, pg. 12-17.

"Multilayer Mosaic Sensing Layers for Infrared-Storage Tubes", M.H. White, M.P. Siedband, S.P. Anderson, E.L. Irwin, Proceedings of IRIS, (Infrared Imaging Symposium), IRIS Conference, Stanford, California, 1964.

"Integrated Structures Utilizing Electric Fields", Vasil Uzunoglu, M.H. White, NAECON Conference, May 11-13, 1964, Dayton, Ohio.

"Molecular Blocks Simplify Microcircuits", Vasil Uzunoglu and M.H. White, Electronics, February 14, 1965, pg. 36-39.

"Maximum Pulse-Repetition Rate for an Injection Laser", Vasil Uzunoglu and M.H. White, Proceedings of the IEEE (Correspondence), 51, June 1963, pg. 960.

NAME: Marvin H. White (Continued)

PUBLICATIONS: (Continued)

"Utilization of Retarding Field Transistors", Vasil Uzunoglu and M.H. White, Proceedings of the IEEE, (Correspondence), 51, March 1963, pg. 495.

"Electron-Beam Scanned IR Mosaic", D.D. O'Sullivan, M.H. White, and M.P. Siedband, Proceedings of IRIS, Conference San Diego, CA 1962.

"Characterization of Microwave Transistors", M.H. White and M.O. Thurston, Solid-State Electronics, 13, 523, 1970.

"A Study Relating MOS Processes to a Model of the Al-SiO_2-Si System", M.H. White, F.C. Blaha, D.S. Herman, Silicon Device Processing Conference, NBS Symposium, June, 1970.

"Investigations of CMOS Surfaces", I.A. Mack, F.C. Blaha, M.H. White, presented at GOMAC 1970, Ft. Monmouth, N.J.

"Charge Distribution in the Multiple Dielectric Structure: P_2O_5:SiO_2", M.H. White, F.C. Blaha, D.S. Herman, presented at the Electrochemical Society 139th Meeting, Spring, Washington, D.C., May 1971.

"Direct Tunneling in MNOS Structures", M.H. White, presented at 31st Annual Physical Electronics Conference (APS), Gaithersburg, Maryland, Spring 1971.

"MNOS Non-Volatile Memory Devices", Distinguished Lecture Series, Ohio State University (October 1971), Columbus, Ohio.

"Characterization of MNOS Memory Transistors", M.H. White, presented at EUROCON 71, Lausanne, Switzerland, October 1971.

"Microminiature Ganged Threshold Accelerometers Compatible with Integrated Circuit Technology", W.D. Frobenius, S.A. Zeitmon, M.H. White, D.D. O'Sullivan, R.G. Hamel, IEEE Trans. on Electron Devices, ED-19, 37 (1972).

NAME: Marvin H. White (Continued)

PUBLICATIONS: (Continued)

"Charge Transport and Storage in High-Speed Complementary MOS Memory Transistors", M.H. White, J.R. Cricchi, presented at International Electron Devices Meeting, October 11-13, 1971, Washington, D.C.

"CCD Imaging at Low Light Levels", M.H. White, D.R. Lampe, F.C. Blaha, I.A. Mack, IEEE International Electron Devices Meeting, December 1972, Washington, D.C.

"Characterization of CCD Line and Area Array Imaging at Low Light Levels", M.H. White, D.R. Lampe, I.A. Mack, F.C. Blaha, IEEE International Solid-State Circuits Conference, February 1973, Philadelphia, Pa.

"Characterization of Thin-Oxide MNOS Memory Transistors", M.H. White, J.R. Cricchi, IEEE Trans. on Electron Devices, ED-19, 1280 (1972).

"Charge Coupled Devices", Electro-physics Seminar Series at University of Maryland (February 1973), College Park.

"MNOS Memory Transistors and Circuits", MNOS Workshop Wright-Patterson AFB, Dayton, Ohio, March 1973.

"An Electrically Programmable LSI Transversal Filter for Discrete Analog Signal Processing (DASP)", D.R. Lampe, M.H. White, J.H. Mims, J.L. Fagan, Proceedings of CCD Applications Conference, San Diego, CA, pp. 111-26, 18-20 September 1973.

"Characterization of Surface Channel CCD Image Arrays at Low Light Levels", Proceedings of CCD Applications Conference, San Diego, CA, pp. 23-26, 18-20 September 1973.

"CCD and MNOS Devices for Programmable Analog Signal Processing and Digital Nonvolatile Memory", IEEE International Electron Devices Meeting, Wash., D.C., (Technical Digest, pp. 130-33), 4 December 1973.

"Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE Journal of Solid-State Circuits, SC-9, No. 1, pp. 1-13, February 1974.

NAME: Marvin H. White (Continued)

PUBLICATIONS: (Continued)

"An Electrically Reprogrammable LSI Analog Transversal Filter", D.R. Lampe, M.H. White, J.L. Fagan, J.H. Mims, IEEE International Solid-State Circuits Conference, Philadelphia, PA, (Digest of Technical Papers: pp. 156-57) 14 February 1974.

"CCD for Discrete Analog Signal Processing (DASP)", D.R. Lampe, M.H. White, J.H. Mims, W.R. Webb, IEEE Intercon 74 (paper 9/2), New York, 26 March 1974.

"Noise Considerations in Solid-State Imagers", M.H. White, D.R. Lampe, IEEE Intercon 74 (paper 2/5), New York, 26, March 1974.

"Nonvolatile Charge Addressed Memories", J.L. Fagan, D.R. Lampe, M.H. White, D.A. Barth, Government Microcircuit Applications Conference, Boulder Colo., 25-27 June 74 (Digest, pp. 194-5).

"A Nonvolatile Charge-Addressed Memory (NOVCAM) Cell", M.H. White, D.R. Lampe, J.L. Fagan, D.A. Barth, IEEE IEDM, Wash., D.C., 9-11 December 1974.

"A Nonvolatile Charge-Addressed Memory (NOVCAM) Cell", M.H. White, D.R. Lampe, J.L. Fagan, D.A. Barth, Lehigh Valley Semiconductor Symp., Bethlehem, PA, 25 April 1975.

"A Nonvolatile Charge Addressed Memory Cell", M.H. White, D.R. Lampe, F.J. Kub, D.A. Barth, IEEE Journal of Solid-State Circuits Special Issue, Oct. 1975.

"Nonvolatile Charge Addressed Memories", D.R. Lampe, M.H. White, J.L. Fagan, National Electronics Conf., Chicago, Ill., 6 October 1975.

"CCD Analog Signal Processing", IEEE Int'l Telemetering Conf., Wash., D.C., 12 October 1975, M.H. White.

"CCD Analog Signal Processing", M.H. White, Int'l Conf. on Applications of CCD's, San Diego, CA, 29 October 1975.

NAME: Marvin H. White (Continued)

PUBLICATIONS: (Continued)

"A High Density, Read/Write, Nonvolatile, Charge-Addressed Memory (NOVCAM)", J.L. Fagan, M.H. White, D.R. Lampe, IEEE International Solid State Circuits Conference, Philadelphia, PA, February 1976.

"An Analog CCD Transversal Filter with Floating Clock Sensor and Variable Tap Gains", M.H. White, I.A. Mack, F.J. Kub, D.R. Lampe, J.L. Fagan, IEEE International Solid State Circuits Conference, Philadelphia, PA, February 1976.

TEXTBOOKS:

Integrated Electronic Systems, Staff of Science and Technology Prentice-Hall, New York (1970).

Semiconductors and Semimetals, Vol. 7a, Semiconductor Applications, MOS Transistors, Marvin H. White, Academic Press, New York, 1970.

SOCIETIES:

Institute of Electrical & Electronic Engineers (IEEE)
Professional Group in Electron Devices (PGED)
Sigma Xi
Maryland Academy of Sciences

NAME: John W. Dzimianski, Advisory Engineer

EDUCATION: B.S. in Electrical Engineering, The Johns Hopkins University, 1947
Dr. Engr. in Electrical Engineering, The Johns Hopkins University, 1952.

EXPERIENCE:

1944 - 1946	Assistant Supervisor, U.S. Army, Radio Section. Installation and maintenance of radio equipment.
1947 - 1952	Research Assistant at the Johns Hopkins University, high frequency electrical insulation and high current arc studies.
1952 - 1956	Allis Chalmers Manufacturing Company, Milwaukee, Wisconsin. Engineering responsibility for electrical laboratory. Responsible for basic electrical research, gaseous electronics, thermonuclear reactors and electronic instrumentation.
1956 - 1959	Westinghouse Electric Corporation, Systems Development Division, Senior Engineer working on infrared systems and integrated circuits.
1959 - 1962	Fellow Engineer: Basic Molecular Program, assistant to project manager and technical director of program.
1962 - 1969	Advisory Engineer - Program Manager - Physics of Failure Program for Semiconductors - ILS Flight Positioning System.
1969 - Present	Advisory Engineer - Technical Director Quality Assurance and Failure Analysis programs for the Solid State Technology Laboratory.

PATENTS: Five patents granted.

PUBLICATIONS: Over 10 publications with emphasis on Microelectronics Reliability.

NAME: John W. Dzimianski (Continued)

SOCIETIES:
IEEE
Electrochemical Society
Tau Beta Pi
Sigma Xi
Eta Kappa Nu

NAME: Chester W. Waldvogel, Fellow Engineer, Computer and Data Systems

EDUCATION: Polytechnic Institute, Baltimore, Maryland, 1936

EXPERIENCE:

1938 - 1942	The Glen L. Martin Company, Tool designing
1942 - 1944	Westinghouse Electric Corporation. Die and electronic package design.
1945 - 1946	Chase Engineering Company, Engaged in the design of various tools and plant layouts.
1946 - 1948	Conlan Design and Engineering, Designed tools, fixtures, machines. Assisted in building designs.
1950 - 1951	Alexandria Iron Works, Structural steel design for buildings and bridges.
1951 - 1953	Machine and Tool Design, Worked on design of tools and dies, wire drawing machinery and the first coaxial cable machine.
1953 - 1954	Mathieson Chemical Corporation. Design Engineer. Duties consisted of the design of a hydrazine plant, including its special handling equipment.
1954 - 1955	Aircraft Armaments, Design Engineer. Design and packaging for a receiver which could be air dropped on either land or water and was triggered from a distance. Design for a training device, housed in a trailer, to simulate radar gun control.

NAME: Chester W. Waldvogel (Continued)

EXPERIENCE: (Continued)

1955 - 1960	The Martin Company, Chief Engineer. Responsible for the Ground Support Equipment on the Titan Program at Cape Canaveral. Conducted R and D contract on ultrasonics for the P6-M aircraft. Participated in the design and manufacture of a simulator for the Pershing missile and the test and checkout equipment for the Titan Program. Group Engineer on P6-M navigation and mine laying system which included the test and checkout of the astrocompass manufactured by General Precision Labs.
1960 - 1962	Electronic Products Corporation, President. Formed and developed corporation which ultimately employed 147 people in the design and manufacture of timing devices. In addition to managing the company, duties included monitoring and assisting in the package configuration of all products.
1963 - Present	Westinghouse Defense and Space Center, Defense and Space Systems Operations, Computer and Data Systems Technology Group, Research and Development (Hybrid). Responsible for the computer development laboratory including technicians, draftsmen, all necessary electronic equipment, calibration, components and storage.

NAME: Roman George Knysh, Quality & Reliability Assurance Manager

EDUCATION: Manhattan College, B.E.E., 1967
Graduate Courses at University of Maryland
Advanced Course on System Safety, George Washington University

EXPERIENCE:

1967 - 1969 Western Union Telegraph Company Design, test and installation of data processing equipment. Involved in development of both message storage and circuit switching systems.

1969 - 1972 Westinghouse Electric Corporation - Engineer. Assisted in the implementation of the reliability and safety programs on the B57G and ECM programs; performed the reliability analysis on the F-15 Radar; responsible for quality and test verification on the MK-27 and MK-48 torpedoes; assisted in the reliability system studies of Program 749; responsible for reliability tradeoffs of CMOS, MOS and plated wire computer technologies; studied the design for the Viking Radar Altimeter; responsible for the engineering and implementation of the safety program on the PAVE SPIKE System; established the quality assurance provisions for the Impact and Proximity Sensors for SAMSO; lead engineer on the research and development programs on reliability of solid state devices.

1972 - 1973 Senior Engineer. Responsible for quality assurance of solid state L-Band transceiver modules; Director of reliability for development of a nonvolatile MNOS memory storage chip for the BORAM module program. Responsible for the reliability and availability tradeoff studies on the Design to Price EW Suite program. This involved system level analyses that considered system complexity, redundancies, environmental factors,

NAME: Roman George Knysh (Continued)

EXPERIENCE: (Continued)

maintainability, and part reliability levels to establish various cost effective systems and configurations.

1973 - Present Quality and Reliability Assurance Manager. Responsible for the quality and reliability of solid state transceiver modules; hybrid power controllers for the Space Shuttle and other experimental space equipment for NASA. Program director of reliability studies on RF power transistors, RF epoxy usage, PROM integrated circuits and Q&RA hybrid technology R&D. Q&RA responsibility for SDD solid state radar programs.

SOCIETIES: Institute of Electrical and Electronic Engineers
Electronic Industries Association - Associate Member - System Safety Committee.

NAME: Thomas G. O'Donnell, Semiconductor Product Lines Manager

EDUCATION: US Naval Academy, Marine Eng'rg. 1957 - 1960
Northeastern University Ind. Eng'rg. 1960 - 1962
Loyola College - currently pursuing MBA program.

EXPERIENCE:

1973 - Present Semiconductor Product Lines Manager, Semiconductor Operations Group, Westinghouse Systems Development Division. Management of all activities of a facility engaged in development and manufacture of complex, custom designed, LSI (Large Scale Integrated) devices for applications in advanced aerospace electronic systems. Annual sales - $10 million. Responsible for production and financial planning and control, budgeting and engineering and manufacturing personnel management. Also responsible for capital investment planning, coordination of new product development, customer liason, and for various management committees.

1969 - 1973 Product Engineering Manager, Semiconductor Operations Group, Westinghouse Systems Development Division. Responsible for supervision of Product, Process, and Test Engineering activities for MOS, MNOS, and complementary micropower Linear devices. Direct activities on new product development-initiate and evaluate programs for cost, performance, and reliability improvements; establish data collection and analysis techniques; supervise projects associated with process development, process control, equipment evaluation and implementation, development of specifications and operating procedures, and cost improvements. Participate in various management, customer liason, contract proposals, and capital expenditures planning.

NAME: Thomas G. O'Donnell (Continued)

EXPERIENCE: (Continued)

1968 - 1969	Product Manager, Custom Product Line Westinghouse Molecular Electronics Division, Elkridge, MD. Responsible for providing technical and administrative leadership to the product line and for planning and executing an annual GSB of $3 million. Had complete P & L responsibility reporting to Operations Manager. Products were special purpose and high reliability types including devices for both Minuteman and Manned Orbiting Laboratory Programs. Developed organizational structure to manage the unique situations present in this specific market; implemented budget, inventory, and production control procedures resulting in a significant improvement in the consistency of monthly billings.
1966 - 1968	Supervisory Engineer, Linear Product Line Westinghouse Molecular Electronics Div. Elkridge MD. Responsible for all line engineering functions covering wafer processing, assembly, electrical test, and environmental screening on complex analog circuits directed at the military and commercial market. Played a primary role in the initial facility setup managing such activities as specification of equipment, conceptual layouts, process and product refinement, etc. Also responsible for section budgets, cost improvement programs, yield improvement programs and for assisting in customer liason and contract negotiations.

NAME: Thomas G. O'Donnell (Continued)

EXPERIENCE: (Continued)	1962 - 1966	Engineer, Manufacturing Engineering Department Westinghouse Molecular Electronics Division, Elkridge, MD. Responsible for setup and control of photomasking, metallization, in-line and wafer test, and associated processes for manufacturing facility. Product engineering responsibility for the Westinghouse 200 Series DTL product line.
	1960 - 1962	Engineer, Research and Development Dept. Transistron Electronic Corp., Boston, Mass. Process development for all phases of fabrication to be utilized on high frequency planar transistors. (2N697 and 2N698)

NAME: Philip C. Smith, Senior Engineer

EDUCATION: BSEE, Carnegie Mellon University, 1966
MSEE, Carnegie Mellon University, 1967
Ph.D.EE, Carnegie Mellon University, 1971

EXPERIENCE:

1966 - 1971	Electrical Engineering Department Carnegie Mellon University, Thesis research on electrical properties of silver doped silicon.
1971 - 1972	Project Engineer, Sensormatic Electronics Corporation. Development of microwave anti-shoplifting system.
1972 - 1975	Scientist, Motorola Semiconductor Division Applied research and process development for MNOS memory and CMOS on sapphire circuits. N channel silicon gate process development.
1975 - Present	Senior Engineer, Westinghouse Electric Corporation. Product engineering for MNOS memory.

PUBLICATIONS: Paper presented at October 1970 meeting of Electro-Chemical Society.

International Journal of Electronics, Vol. 30, (1971), p. 255 and Vol. 32, (1972) p. 697.

SOCIETIES: IEEE

NAME: Lawrence Epstein, Senior Engineer

EDUCATION: B.S. in Chemistry, Brooklyn College, 1955. Graduate courses in Chemistry, Metallurgy and Semiconductor Device Technology

EXPERIENCE:

1972 - Present Westinghouse Electric Corporation Systems Development Division Baltimore, Maryland

1957 - 1966 Ronson Metal Corp., Newark, N.J. Chief Chemist and Manager Special Products. Production and quality control of rare earth metals and alloys.

1966 - 1972 RCA, Solid-State Division, Somerville, N.J., Engineer, Process engineering for diffusion, photoengraving and metallization of IC's. Member of manufacturing engineering staff for "SAFEGUARD" program. Later developed manufacturing process for low voltage COS/MOS devices. At Solid-State Technology Center, Advanced Development Pilot Line, involved in developing processes for 1024-bit P-MOS and 256-bit COS/MOS memories and high voltage, high current bipolar arrays including dielectric isolation.

1972 - Present Westinghouse Systems Development Division, Advanced Technology Laboratories. Lead engineer for process engineering for pilot lines producing products such as CMOS multi-metal arrays, complementary bipolar IC's, p-channel silicon gate arrays and MNOS memory arrays.

PUBLICATIONS: "Analytical Control of Rare Earth Products," Stevens Institute of Technology, 1965.

"Materials for and the Mechanism of Gettering Multiple Component Gases", AFCRL-63-7, 1963.

"Dimensional Control in Photoengraving," Kodak Microminiaturization Seminar, May 1970.

NAME: Gard Lee Poward

EDUCATION: BSIE Pennsylvania State University 1965

EXPERIENCE:

1966 - 1967	Westinghouse Electric Corporation, Aero Space and Electronic Systems Division. Industrial Engineering administrating the Measure Day Work System in the Inductive Components Fabrication Area. Provided detail plans for measuring and controlling manufacturing performance, manufacturing method studies, compiled schedule, and performance appraisal.
1967 - 1971	Manufacturing Engineer. Worked in Manufacturing R&D Methods Group developing tooling, processes, and assembly techniques for Multickys Hybrid Packages (MHP's).
1971 - 1972	Manufacturing SDD Program Manager. Responsible for all facets of fabrication assembly, test, and manufacturing planning for Skylab. Television System.
1972 - Present	Manufacturing SDD Program Manager for Solid State Microwave MHP's.

APPENDIX A
ARMY/NAVY MNOS BORAM

76-1008

Army/Navy MNOS BORAM

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Army/Navy MNOS BORAM

J.E. Brewer, E.J. Gallagher, and F.A. Phillips

Abstract - An advanced development model of an MNOS BORAM module and evaluation results to date are described. This class of memory meets military needs for general purpose computer secondary storage. It is a superior and cost effective alternative to fixed head electromechanical storage.

INTRODUCTION

The growth of electronic data processing in many military applications has been hampered by inadequate memory capacity. The traditional secondary memory approach involving fixed head electromechanical storage leads to compromises of reliability and performance which are often unacceptable. The metal-nitride-oxide-semiconductor (MNOS) technology offers a nonvolatile solid-state memory alternative which avoids those compromises.

The feasibility of the MNOS approach has been demonstrated by the design, fabrication and evaluation of a computer secondary storage module. This advanced development was carried out by the Westinghouse Electric Corporation under the joint sponsorship of the Army Electronics Command (ECOM) and the Naval Air Systems Command (NASC). Initial module evaluation was conducted at the Naval Air Test Center (NATC), and additional evaluations at ECOM are in progress.

In a sense, this is a status report. Both the development and evaluation activities are still underway, and will continue for several years. The discussion here is limited to the storage system. The MNOS memory component will be treated in other publications. This paper describes the advanced development model and discusses evaluation results to date.

SYSTEM CONCEPTS AND OBJECTIVES

The objective of the MNOS BORAM development effort was to provide a cost effective block-oriented random access memory suitable for use as a general purpose militarized computer secondary storage unit.

In a modern computer system, the memory is a dominate factor in determining system hardware cost and reliability. As shown in figure 1, memory is usually organized in a hierarchial fashion to achieve required capacity and performance at a tolerable cost. Primary memory is randomly word addressable. It provides fast data access, and is relatively expensive. Secondary and higher order memory may be addressable in a different fashion. Higher levels have progressively larger capacity, slower access and lower cost. Hierarchy design involves tradeoffs at each level of access time, capacity and cost to achieve global objectives such as maximum computer throughout per dollar.

To facilitate processing, a popular approach is to partition data and program into fixed groups of words called a "page". The assignment process may not be visible to the user. Pages which contain data and program for immediate processing reside in primary memory. When the computer cannot find a required item in primary memory, a page fault is said to have occurred. In this event higher order memory must be referenced to obtain the necessary page or pages, and the processing of the related program must be terminated until the data is available in primary memory.

Computer idle time because of delay in obtaining data from high order storage affects system productivity. Reduction of idle time is a major theme in both software and hardware design. The simultaneous execution of input/output (I/O) operations and computing operations is a key design strategy. Multiprogramming schemes where a computer keeps pages from several programs in main memory and jumps from program to program when I/O is necessary, is another important approach. A considerable software overhead burden is encountered to keep track of data and current operations.

The performance of a secondary storage unit is primarily characterized by the required time delay between reception of a request for a data block and the time when the block is available in main memory. This time can be conveniently partitioned into access time and flow time.

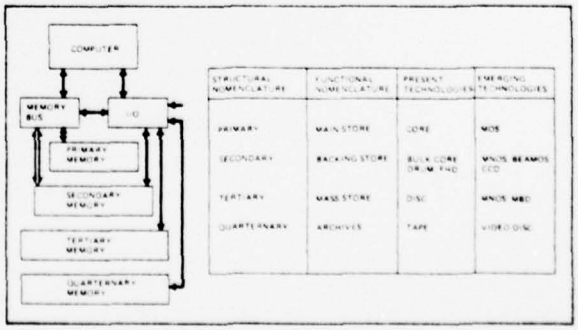

Figure 1. Computer System Memory Hierarchy

Access time is the delay between the reception of the request and the availability of the first data element of the block at the data port of the storage unit. Flow time is the time required to transfer the entire block from the data port to primary memory.

A preferred organization for secondary storage is block-oriented random access memory (BORAM). By definition, a random access memory can access the contents of any address within a fixed time. This access time is uniform for all elements, and is independent of the order of addressing. Block orientation is preferred because it most efficiently accomplishes the task of providing needed pages. BORAM organization can significantly reduce both hardware and software complexity.

Secondary storage approaches based on rotating electromechanical components or circulating shift registers are inherently block oriented, but do not met the random access criteria. For these technologies, a rotational latency exists which causes an uncertainty in the access time. Hardware must incorporate timing and sensing circuitry to keep track of rotational position. To reduce the impact of latency, software systems must consider rotational position as a parameter for servicing I/O ques.

The development objective of providing a "general purpose" secondary storage unit is much easier to achieve given a BORAM organization. "General purpose" implies that the storage unit can be used with different computers of varied characteristics with only minor software and hardware adjustments. Rotating or circulating storage will require some type of special controller for computer interface. In contrast a BORAM will need only to be made compatible with the computer system interface levels and protocol.

An important part of the BORAM development objective was "cost effectiveness". It is relatively easy to compare MNOS BORAM against alternative technologies on a parameter by parameter basis. It is more difficult to place the proper relative value on individual parameters. In commercial computing applications major emphasis is placed on cost. For military use reliability, power dissipation, cooling requirements, volume and weight assume great importance. Maintenance, spares, documentation and training costs over the lifetime of the equipment should be considered. Cost effectiveness can only be determined in the context of a specific application. There are reasons to believe that the reliability and modularity of MNOS BORAM will be reflected in low life cycle costs. Studies have just been initiated to explore this area.

MODULE DESCRIPTION

The advanced development MNOS BORAM module shown in figure 2 is a self contained general purpose secondary storage unit. No external controllers or power supplies are required for operation. It has very low power dissipation and no special cooling arrangements are necessary. The design is all electronic. The historic electromechanical storage problems with moving parts, vacuum systems, moisture and dust particles are avoided. Data access delay time is more than 100 time better than the fastest drum. No rotational latency time exists. Flow rates match the maximums allowed by computer system interface specifications. The module mechanical design demonstrates volume and weight advantages over comparable fixed head magnetic systems. In addition, the highly modular nature of the design contributes to ease of interfacing and to economics in logistics.

This first BORAM module has been a vehicle for learning about the MNOS technology. Evaluations at the Naval Air Test Center have confirmed that the advantages claimed above are real. The advanced development effort has accomplished its limited objective of demonstrating technical feasibility.

It must be pointed out that only items appropriate for advanced development and essential to demonstration of technical feasibility were initially funded. The initial October 1975 delivery

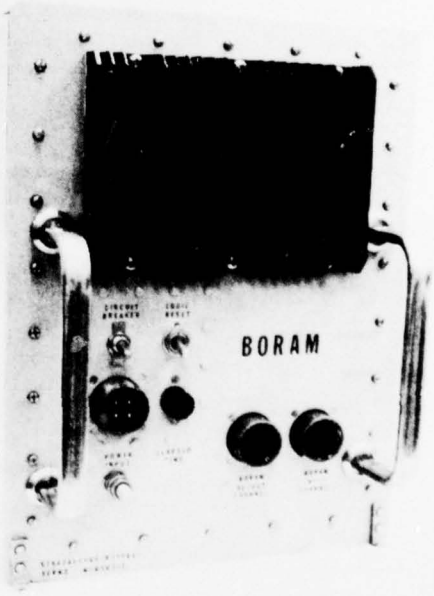

Figure 2. A Front View of the MNOS BORAM Module Advanced Development Model

configuration of the module was 1/64 populated. System level environmental tests have not been performed. Further production experience and engineering development is needed. Computer system benefits in terms of performance and life cycle costs need to be better quantified. In the near future it is expected all of these open issues will be addressed.

Devices are currently being manufactured to expand the memory to the full complement of 16.8 megabits. Module design anticipated the military environment even though system environmental tests have not been performed. Individual components including the memory chips operate over the -55°C to +125°C temperature range. The modified full ATR case design included provisions for EMI control.

Table 1 and figure 3 summarize the salient aspects of the module. Individual characteristic parameters will be discussed in the text below. The four block functional diagram shows the simplicity of the design, and should aid in understanding module operation.

Table 1. Major Characteristics of the MNOS BORAM Advanced Development Model

CHARACTERISTIC	MAGNITUDE	UNITS
Storage Capacity	524,288	32 bit words
Read Access Time	30	microseconds
Data Transfer Rate	250,000	words/sec
Data Retention Time	4,000	hours
Volume	1.48	cubic feet
Weight	105	pounds
Module Power	100	watts

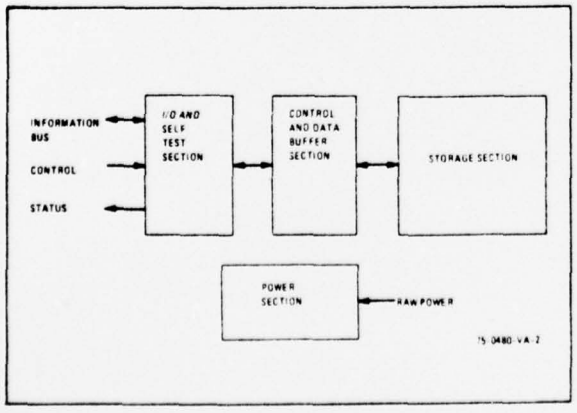

Figure 3. BORAM Module Functional Block Diagram

An I/O section (1 card) provides the function of interfacing to a particular computer system. Drivers, receivers, and interface protocol logic are implemented here. Any logical feature that is likely to be a function of a particular computer system is included. Self test is an example. Data format conversion is another case. The I/O section is an intermediary between an external computer and the module control section.

A control section (1 card) conducts all data transactions in response to I/O section requests. It contains circuitry to control the operation of the storage section. It contains a data buffer, a data encoder, and error detection and correction circuitry.

The storage section (32 cards) constitutes the largest part of the module. Taking advantage of the nonvolatile nature of MNOS, the memory cards are normally powered down. A card consists primarily of memory chips with a small complement of decoding, power switching and buffering circuitry.

A BORAM module is a slave to a computer. The computer initiates and directs transactions. To perform a read, the computer would signal to the I/O section. The I/O section would interpret the signals, place the control section in the read mode, and request a word from the data buffer. The computer would take the data from the BORAM module at its own asynchronous rate using an appropriate interface protocol.

In response to I/O section requests the control section will act to maintain a reservoir of words in the data buffer. It will power up the addressed memory card and read data from storage to the data buffer until the buffer is full. This is a relatively high speed synchronous transaction which minimizes the duty cycle of the storage section. Between accesses the storage section is powered down. Because of interlaced timing, data may be taken from the buffer at anytime.

The fourth functional block in figure 3 is the power section. The advanced development model operates from a 120/208 Vac 3-phase wye connected 400-hertz power source. The power section provides 7 different regulated and protected dc voltage levels. The total dc load is 35 to 40 watts. Because of supply inefficiency, the ac power to the module is 85 to 100 watts.

MODULE PERFORMANCE

A BORAM module serves as a slave to a computer. Module operation involves both hardware and software interaction. Therefore, a discussion of performance must be couched in the context of a host data processing system. Currently

the advanced development model is equipped with two different I/O cards. One card allows communication with US Navy NTDS (ANEW) computer interfaces (MIL-STD 1397 Type C computer interface). A second card is oriented toward the US Army AN/GYK-12 (TACFIRE) interface.

Personnel at the Naval Air Test Center have used the BORAM with the NTDS I/O card for approximately one year. The unit has been successfully operated with a PDP11/45 computer in the NATC Systems Engineering Latoratory. Extensive observations of performance of the module and the memory components were carried out at this site. The module was also operated successfully with the CP642B computer located at the NATC Chesapeake Test Range. In this case configuration controlled NTDS software was developed to allow references to the BORAM. Demonstration programs were prepared where NTDS operational programs were sourced from BORAM instead of core memory.

The more salient aspects of BORAM performance were readily confirmed. The BORAM operating protocol was observed and found to conform to NTDS specifications. In practice, however, the module responses were so much faster than the computer that throughput was limited by the computer. By operating with a test tool, it was shown that reading and writing could be accomplished at the maximum allowed interface rate of 250,000 words per second. Access time to the first word of a data block was measured as 26 microseconds. This was 4 microseconds less than the 30 microsecond objective shown in table 1. This is two to three orders of magnitude faster than comparable drum or fixed head disc systems.

For the NTDS interface, the BORAM responds to six instructions: STOP, READ, WRITE, STATUS, RESET and TEST. Figure 4 shows the instruction word format. The manner by which an individual instruction is executed is determined by the modified bits in the instruction word.

M4 Suppress timeout termination
M3 Suppress error correction
M2 Stop at group boundary
M1 Stop at block boundary
M0 Increment address

Bit No.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbols	C2	C1	C0	M4	M3	M2	M1	M0	X	B7	B6	B5	B4	B3	B2	B1	B0	G3	G2	G1	G0	X	X	
Name	Operation Code			Modifier Field					Spare	Block Address								Group Address				Spare		
										Address Field														

Figure 4. BORAM Instruction Word Format for NTDS (ANEW) Interface

Considerable flexibility is allowed in addressing. The module will recognize a "group" or a "block". A group is composed of 128 words, and a block contains 2048 words. The module storage capacity can be expressed in various units.

256 blocks
4096 groups
524,288 words
2,097,152 bytes
16,777,216 bits

As implied by the acronym BORAM, groups and blocks can be addressed in random order. Each of these data sets consists of an ordered sequence of 32-bit words. Operations always begin with the first word in the data set. A read or write may be terminated by the computer at any time without loss of information.

PACKAGING AND MODULARITY

Adequacy of packaging and modularity concepts have far reaching consequences on the suitability and ultimate cost of a memory system. MNOS BORAM has significant potential for dense cost effective packaging. The advanced development effort explored some of this potential with impressive results.

Figure 5 presents the packaging concept for the first module. The module is composed of six discrete assembly items: memory cards (32), I/O card, control card, backplane, chassis structure, and front panel. All items are readily accessible for replacement. Each assembly can be produced, tested and inspected as a unit before module assembly. The respective items are reasonably independent in a functional sense, and have simple well known interfaces. This implies that each item can be optimized for producability without forcing changes in the other items.

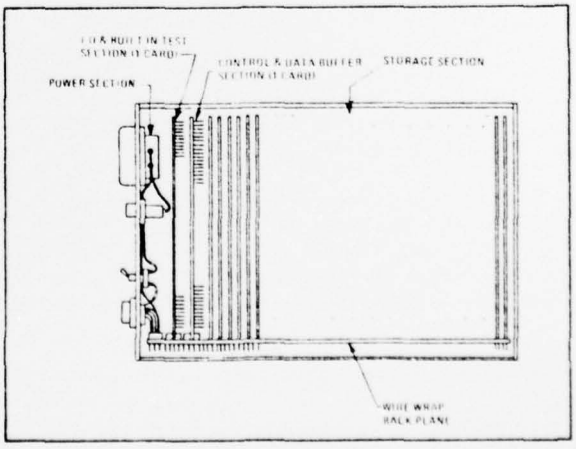

Figure 5. BORAM Module Packaging Concept

A primary goal of the mechanical partitioning was to provide economy in logistics and in volume production. A production version of the BORAM should be usable by all three services in many different programs. Common usage items would include the memory cards, control cards, backplane and chassis structure. Items which would vary for different subgroups of users include the I/O card and front panel.

The module is housed in a modified full ATR box which is 10.125 inches wide, 19.5625 inches deep, and 12.9 inches high. Table 2 summarizes module packaging density parameters. Information density calculations are referenced to the data bits actually available to the user. Data is stored in 38-bit words which consist of 32 information bits and 6 redundancy bits. Therefore, the effective bits per chip are 32/38 of the actual bits per chip.

Table 2. Density Parameters for the Advanced Development Model of the MNOS BORAM

CHARACTERISTIC	TOTAL MODULE	POWER SECTION & FRONT PANEL OMITTED
SYSTEM		
information bits	16.8 megabits	16.8 megabits
volume	2555 in^3	2142 in^3
mass	105 lb	95 lb
power	100 watts	40 watts
number of chips	9728 chips	9728 chips
INFORMATION DENSITY		
bits/chip (effective)	1725	1725
bits/cm^3	401	478
bits/gram	352	389
mwatts/bit	5.96	2.38
PACKAGING DENSITY		
cm^3/chip	4.30	3.61
grams/chip	4.90	4.43
mwatts/chip	10.28	4.11
grams/cm^3	1.14	1.23

The information density for the BORAM module was surprisingly good considering that the memory component contains only 2048 bits. A typical militarized drum might achieve 50 bits/cm^3 and 90 bits/gram. One particular fast access fixed head disc achieves 266 bits/cm^3 and 301 bits/gram. The same unit running at one half speed can increase the density to 466 bits/cm^3 and 528 bits/gram.

It was concluded that MNOS BORAM based on 2048-bit chips can compete well in information density with fixed head systems. MNOS BORAM based on larger chips should achieve very significant density advantages over fixed head systems.

The use of multichip hybrid integrated circuitry in the storage section allowed the achievement of high density. Figure 6 shows the 16-chip microcircuit and the memory card. A memory card contains 608 chips and stores 16,384 words where each word contains 38 bits. The board is

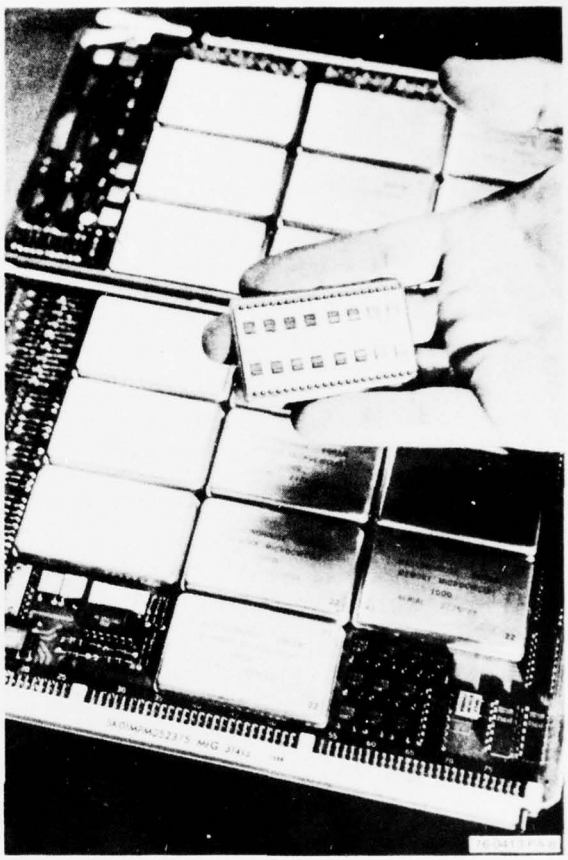

Figure 6. MNOS BORAM Memory Card and Memory Microcircuit

9.5 inches wide and 12.0 inches high. The module storage section accommodates 32 memory cards on 0.45-inch centers.

The low power dissipation required for module operation allows the use of conduction for internal heat transfer. Cards are designed for low thermal impedance to the sidewalls of the ATR case. No moving air or liquids are required. Unreliable power hungry fans are avoided. The power supply with an internal dissipation of 50 to 60 watts is the largest heat generator in the module. It is mounted in good thermal contact with the front panel. Fins are provided on the front panel to insure adequate heat transfer to external ambient air. Thermocouple measurements on the power supply case show temperatures less than 15°C above the room ambient. Temperatures in the storage section remain within a few degrees of room ambient.

DIAGNOSTIC CAPABILITY

In a storage system, the accuracy of the data must be assured. The computer must somehow

be informed of memory malfunctions, and means must exist for rapid fault isolation or diagnosis of problems. It must also be anticipated that maintenance philosophy and capability may vary widely between users. This latter point is important because the BORAM is intended for many diverse applications.

The advanced development BORAM module included several features to avoid undetected errors, and to aid in fault isolation. Circuitry was provided to check the data and give an alarm in the event of errors. The status of the dc power levels within the BORAM are also monitored, and an alarm signal is emitted in the event of serious deviation. Built-in test features are incorporated in the form of four test instructions. Test may be conducted by the computer or by maintenance test tools.

The manner by which malfunctions are reported is of course a function of the host computer. For the NTDS (ANEW) interface a status word is provided. The bits in the word keep track of internal failures, illegal transactions, and the manner by which operations were terminated. Status words are sent to the computer automatically in the event of a failure, or on demand in response to a STATUS instruction. The automatic response is accomplished by the BORAM using the NTDS interrupt signaling sequence. The BORAM will continuously send interrupts until the fault condition is removed.

Data error detection is based on the use of a Hamming single-error correction code. Data to be written is received in 32-bit words. Each word is encoded into a 38-bit word before storage. When the data is read from storage it is checked and decoded. If a single-bit error occurs an error alarm signal is generated. This causes an error counter associated with the status word to increment. The single-bit error is corrected before it is transmitted to the computer.

Single-bit errors are the most likely type of failure in the module. Because of error correction this failure can be tolerated without interrupting system operation. The occurrence of the failure is recorded in the error counter. When the error counter over flows, interrupt signals are sent to the computer. In this manner, the BORAM can be flagged for maintenance at the first convenient moment.

The test instructions allow the computer or a test tool to rapidly confirm the internal logic and data paths within the BORAM. Four tests called A, B, C and D are provided. Figure 7 shows how the data paths relate to the functional parts of the BORAM module.

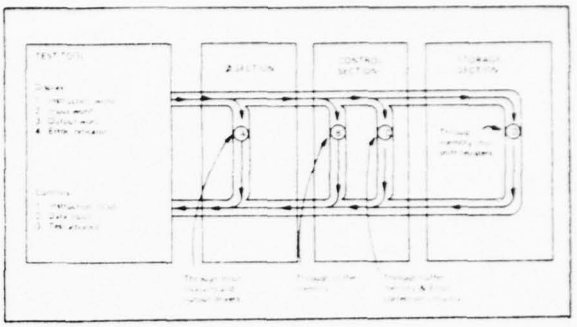

Figure 7. Test Instruction Data Paths Selected by Modifier Bits

Test A verifies that the I/O section logic which interprets instructions and routes data is operational. The communication links between the host computer and the BORAM are checked. Data received by the BORAM is routed to output drivers and sent back to the computer. The computers must generate the data patterns and compare transmitted to received data.

Tests B, C and D continue this process and progressively extend the verified area deeper into the module. Test D actually routes data out to every memory chip in the module.

Computer diagnostic routines can make use of the test instructions, the built-in error detection, and the normal write and read instructions to throughly explore the module. An instruction modifier bit is provided to allow suppression of error correction. With error correction suppressed, the computer can faul isolate to the chip level.

RELIABILITY CONSIDERATIONS

For military applications drum and fixed head disc systems have been avoided because of poor reliability. The MNOS BORAM approach promises almost an order of magnitude improvement in MTBF with no maintenance. In addition, the all electronic solid-state module will tolerate exposure to relatively hostile environments.

MNOS is a metal-insulator-semiconductor integrated circuit technology similar to conventional MOS. It shares the same reliability advantages and problems as MOS. Failure rate experience from MNOS parts in actual field systems has been on a par with MOS experience. The significant difference between MOS and MNOS lies in the nonvolatility of data storage.

A primary strategy in large nonvolatile memor design is to exploit the difference between active chip failure rate (λa) and dormant chip failure

rate (λ_d). An active chip has voltages applied, and electric field stresses exist within the die. A dormant chip has all voltages removed, and electric field stresses within the die are greatly reduced. The failure rate of an active MNOS memory chip is expected to be less than one failure per 10 million hours. The dormant failure rate is much less than the active failure rate, and can be conservatively estimated as one tenth of the active rate.

In a BORAM module all memory chips are normally powered down. Devices are turned on only for a data transaction. In the advanced development model no more than 38 chips are ever turned on at one time. These groups of 38 chips are called segments. For mathematical analysis, a module is said to contain D_m die/module, D_s die/segment and S segments/module.

Figure 8 shows a reliability model block diagram for the BORAM module. To examine the impact of nonvolatility on reliability, the fifth block composed of only the stroage elements will be examined. Table 3 shows equations for four design alternatives. The storage element reliability P_5 is developed from the Poisson distribution for the choice of volatile and nonvolatile semiconductors with and without single-error correction. A numerical solution of these equations is provided in figure 9 for the MNOS BORAM advanced development model.

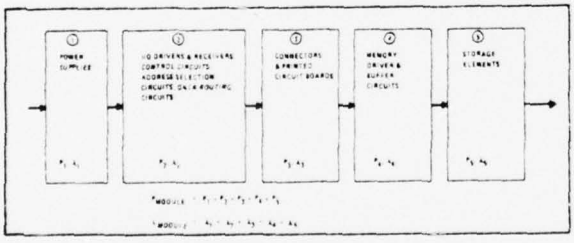

Figure 8. BORAM Module Reliability Block Diagram

Table 3. Storage Element Reliability Equations

MEMORY DEVICE	RELIABILITY EQUATION	
	NO ERROR CORRECTION	WITH ERROR CORRECTION
VOLATILE		
NONVOLATILE		

It is shown that for memories with a large component count volatile technologies are at a serious disadvantage. The preferred choice is clearly a nonvolatile device with error correction. This choice effectively removes the memory component as the major factor in determing system reliability. When the effects of P_1 to P_4 are considered it still appears reasonable to achieve effective MTBF's on the order of 10,000 hours.

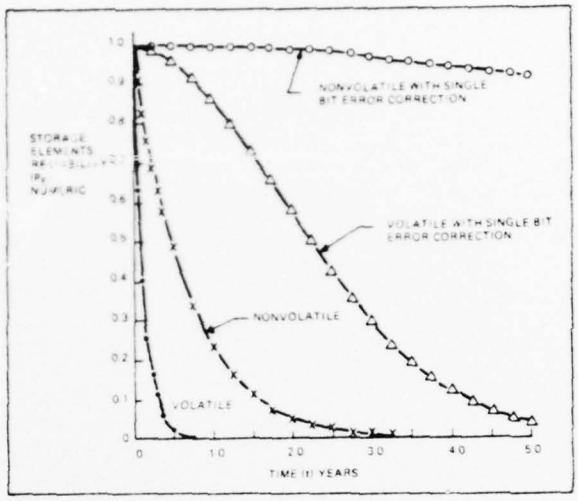

Figure 9. Comparison of Storage Element Reliability for Four Design Alternatives

Nonvolatility, of course, has other more obvious reliability implications. Because the memory chips are powered down, low system power is required. Internal heating is minimal and junction temperatures are quite low. Power supply stresses and complexity are reduced. In short, nonvolatility of the storage enhances the reliability of the other components in the module through a reduction of stress levels.

COST POTENTIAL

Because of the simplicity of the MNOS memory cell, potential exists for very high density memory components. This potential will ultimately result in the commercial application of MNOS BORAM as an alternative to drums and fixed head discs. BORAM will also compete well against some of the smaller high performance moving head systems.

Figure 10 shows the results of a cost projection for military systems performed in 1974. This curve shows total system purchase price versus time through 1990. Currently the technology is immature and prices are relatively high. During the 1980's prices will drop below that of most fixed head systems. Price reductions will occur because of production learning experience, and because of increases in the number of bits per chip. The timing of price decreases can be accelerated or retarded by the availability of funding for engineering development.

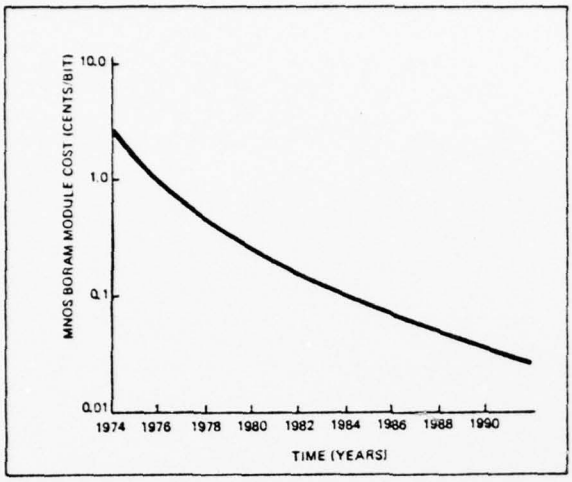

Figure 10. Expected Cost Trend for BORAM Modules

Initial purchase price is only a part of the cost of a storage system. Logistics support costs over the useful life of the unit should also be weighed. Compared to electromechanical systems, MNOS BORAM is expected to offer extended life, simplified maintenance and training, and reduced spares cost. These issues are being studied, and quantified data will soon be established.

SUMMARY

The text has provided a progress report on an advanced development investigation into the technical feasibility of MNOS BORAM as a general purpose militarized secondary storage unit. The vehicle for the investigation was a 16.8 megabit advanced development model. The unit was designed and fabricated by a contractor, and was subjected to an independent government evalulation.

The performance and physical characteristics of the module were verified by direct measurements. The system was interfaced to several host computer systems and was observed to perform well. The unit was shown to be compatible with standard military hardware and software. Data flow rates were observed to match the maximums allowed by interface specifications. Access times of less than 30 microseconds were confirmed. The modular high density packaging of the module was suitable for use in military environments, and was conductive to reduced logistics costs. Built-in diagnostic capabilities will allow simplified maintenance procedures. The nonvolatile nature of the semiconductor memory component contributes significantly to reliability enhancement. Cost projections shown rapid price reductions as development proceeds.

It has been concluded that the technical feasibility of MNOS BORAM has been satisfactorily demonstrated. The technology is a superior alternative to fixed head electromechanical storage, and is capable of meeting military secondary storage needs over a wide range of applications.

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